1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

X260 MLB - CBB

LAST_MODIFICATION=Thu Sep 10 15:22:41 2015

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62	100	page102	J43_MLB	10/24/2012
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ALIASES RESOLVED

PRODUCT SAFETY REQUIREMENTS:
PCB, UL RECOGNIZED, MIN. 130-C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94.
PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP. RATING AND V-0 FLAME RATING.

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-00532	1	SCHEM,MLB,X260	SCH	CRITICAL	
820-00244	1	PCBF,MLB,X260	PCB	CRITICAL	

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Apple Inc.

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BOM Groups

BOM GROUP	BOM OPTIONS
MLB_COMMON	ALTERNATE,COMMON,MLB_MISC,MLB_DEBUG:ENG,MLB_PROGPARTS,BUILD:CBB
MLB_MISC	CAM_FREQ:24M,CAM_XTAL:NO,SSDRAM:4GBIT,S3X:B0,UPC:A1,PCH24M:SUS,EQ:4CH,PMIC:A0D,BSSB_GPIO
MLB_DEBUG:ENG	DEBUGLED

CPU DRAM SPD Straps

BOM GROUP	BOM OPTIONS
DRAM:SAM_8GB	RAMCFG0_L,DRAM_TYPE:SAMSUNG_8GB
DRAM:HYN_8GB	RAMCFG0_L,RAMCFG1_L,DRAM_TYPE:HYNIX_8GB
DRAM:ELP_8GB	DRAM_TYPE:ELPIDA_8GB

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00084	1	IC,SPI SERIAL FLASH,8MBIT,3.0V,CSP,8P	U3090	CRITICAL	UPCROM:BLANK
341S00466	1	IC,NVM (VXXX) CBB, X260	U3090	CRITICAL	UPCROM:PROG
338S1231	1	IC,SMC12-B1,40MHZ/50DMIPS MCU,7X7,168BGA	U5000	CRITICAL	SMC:BLANK
341S00431	1	IC,SMC-B1,EXTERNAL (V2.33A2) PROTO 1,X260	U5000	CRITICAL	SMC:PROG
335S1009	1	64 MBIT SPI QUAD I/O FLASH,CSP,3.3V,QUAD IO	U6100	CRITICAL	BOOTROM_WIN:BLANK
335S1010	1	64 MBIT SPI QUAD I/O FLASH,CSP,3.3V,QUAD IO	U6100	CRITICAL	BOOTROM_MAC:BLANK
335S1029	1	64 MBIT SPI QUAD I/O FLASH,CSP,3.3V,QUAD IO	U6100	CRITICAL	BOOTROM_MIC:BLANK
341S00465	1	IC,EFI ROM (VXXX) CBB,X260	U6100	CRITICAL	BOOTROM:PROG

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00207	1	IC,CPU,SKY,SR2EN,PRQ,D1,2/2,1.1,5W,.85,B1515	U0500	CRITICAL	CPU:1.1GHZ
337S00208	1	IC,CPU,SKY,SR2EM,PRQ,D1,2/2,1.2,5W,.85,B1515	U0500	CRITICAL	CPU:1.2GHZ
337S00209	1	IC,CPU,SKY,SR2EH,PRQ,D1,2/2,1.3,5W,.85,B1515	U0500	CRITICAL	CPU:1.3GHZ
946-3892	1	J11/J13 MLB DYMAX ADHESIVE 29993-SC 0.4G	GLUE	CRITICAL	
825-00162	1	LABEL,BARCODE,2D,1D,CONFIG,MLB,X260	LABEL		

DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S00052	2	IC,SDRAM,LPDDR-1866,32GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S00053	2	IC,SDRAM,LPDDR-1866,32GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S00054	2	IC,SDRAM,LPDDR-1866,32GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:ELPIDA_8GB

CPU DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 3	CFG 2
2GB	0	0
4GB QDP	0	1
4GB DDP	1	0
8GB	1	1

SSD Configs

BOM GROUP	BOM OPTIONS
SSD:128GB	NAND:64GB,CAPACITY1
SSD:256GB	NAND:128GB,CAPACITY0,CAPACITY1
SSD:512GB	NAND:256GB,CAPACITY2
SSD:256GB_SAND	NAND:128GB_SAND,CAPACITY0,CAPACITY1,SANDISK_1Y
SSD:512GB_SAND	NAND:256GB_SAND,CAPACITY2,SANDISK_1Y

SSD Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00175	1	IC,S3-X,B0	U8600	CRITICAL	S3X:B0
333S00017	1	IC,LPDDR3-1600,128MX8,1.8V,25NM,276 POP	U8600_POP_DRAM	CRITICAL	SSDRAM:4GBIT
335S1030	2	NAND,TOG DDR2,2CH,64GB,1YNM,3.3V,LGA60	U9100,U9120	CRITICAL	NAND:64GB
335S00050	2	NAND,TOG DDR2,2CH,128GB,1YNM,3.3V,LGA60	U9100,U9120	CRITICAL	NAND:128GB
335S00051	2	NAND,TOG DDR2,2CH,256GB,1YNM,3.3V,LGA60	U9100,U9120	CRITICAL	NAND:256GB
335S00121	2	NAND,TOG DDR2,2CH,128GB,1YNM,3.3V,LGA60	U9100,U9120	CRITICAL	NAND:128GB_SAND
335S00122	2	NAND,TOG DDR2,2CH,256GB,1YNM,3.3V,LGA60	U9100,U9120	CRITICAL	NAND:256GB_SAND

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00660	1	IC,CD3215,USB PWR SWITCH,A1,6X6MM,BGA96	U3100	CRITICAL	UPC:A1
338S00168	1	IC,PMU,P650839A0D,7X7MM,BGA168	U7800	CRITICAL	PMIC:A0D

Board IDs

BOM GROUP	BOM OPTIONS
BUILD:PROTO1	BOARDID0_L
BUILD:CBB	BOARDID1_L

Board ID should start all-high (first build), and each new build increment stuffing in a binary fashion (ID0 is the LSb). IDx is high if not set low in the BOM table.

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S00074	376S0855		ALL	Toshiba alt for Diodes dual
376S1129	376S0855		ALL	NXP alt for Diodes dual
376S1089	376S1128		ALL	NXP alt for Diodes single
138S0703	138S0648		ALL	Murata alt to Taiyo Yuden
372S0186	372S0185		ALL	NXP alt to Diodes
376S1053	376S0604		ALL	Diodes alt to Fairchild
107S0249	107S0251		ALL	TFT alt to Cyntec
128S00044	128S00041		ALL	Rubycon alt to Sanyo
740S00004	740S0134		ALL	Kemet alt to Sanyo
740S00005	740S0190		ALL	Polytronics alt to Wayon
128S0296	128S0487		ALL	Sanyo alt to NEC
128S00012	128S0487		ALL	ROHM alt to NEC
128S0397	128S0325		ALL	Kemet alt to Sanyo
107S00070	107S0085		ALL	TDK alt to Murata
376S00007	376S1179		ALL	AOS alt to Vishay
376S1080	376S0820		ALL	Diodes alt to OnSemi
152S00311	152S2037		ALL	Cyntec new alt to Cyntec
152S00098	152S00224		ALL	Vishay alt to Cyntec
128S00021	128S00020		ALL	ROHM alt to NEC
138S0786	138S0705		ALL	Samsung alt to Murata

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S00007	128S00015		ALL	NEC alt to Sanyo
128S00009	128S00015		ALL	Kemet alt to Sanyo
128S00029	128S00015		ALL	Rohm alt to Sanyo
128S00011	128S00010		ALL	Kemet alt to Sanyo
128S00026	128S00010		ALL	NEC alt to Sanyo
128S00031	128S00010		ALL	Rohm alt to Sanyo
138S00073	138S00047		ALL	Murata alt to Taiyo
138S0772	138S00013		ALL	Taiyo alt to Murata
132S00012	132S0401		ALL	Multi alt to Taiyo
152S00028	152S1751		ALL	Murata alt to Taiyo Yuden
353S00712	353S2216		ALL	OnSemi alt to TI
353S00714	353S2208		ALL	ONSemi alt to TI
337S00174	337S00175	S3X:B0	ALL	S3X B0 alt to A0
138S00077	138S00035		ALL	Taiyo alt to Murata
152S00343	152S1682		ALL	Murata alt to Cyntec
155S00155	155S0441		ALL	TDK alt to Murata
155S0741	155S0361		ALL	Murata alt to TDK
155S00165	155S0382		ALL	Taiyo alt to TDK
155S00166	155S0391		ALL	TDK alt to Murata
155S0706	155S0302		ALL	Taiyo alt to Murata
197S00053	197S00050		ALL	Kyocera alt to TXC
197S00055	197S00050		ALL	Murata alt to TXC
311S00004	311S0370		ALL	OnSemi alt to NXP
333S00030	333S00016		ALL	Hynix alt to Micron
338S00175	338S1264		ALL	Broadcom alt packaging
107S00020	107S0276		ALL	TFT alt to Cyntec
107S00021	107S0284		ALL	TFT alt to Cyntec
353S00773	353S4296		ALL	Semtech alt to TI
311S00057	311S0612		ALL	Diodes alt to NXP
155S00011	155S00008		ALL	Murata alt to TDK
138S0739	138S0706		ALL	Samsung alt to Murata
138S0945	138S0706		ALL	Kyocera alt to Murata
138S00090	138S0943		ALL	Taiyo alt to Murata
138S00087	138S1086		ALL	Taiyo alt to Murata
107S00086	107S00056		ALL	TFT alt to Cyntec
152S00347	152S00220		ALL	Chilisin alt to Cyntec
138S00032	138S0831		ALL	Taiyo alt to Murata
138S00049	138S0831		ALL	Kyocera alt to Murata
152S00362	152S1129		ALL	Cyntec alt to Murata
128S00039	128S00038		ALL	NEC alt to Kemet

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BOM Configuration [2]

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Top level BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-6664	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 256G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,SSD:256GB,WIFI:FCC
639-6665	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 512G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,SSD:512GB,WIFI:FCC
639-6666	PCBA,MLB,1.3GHZ,HY 8GB,TOSH 256G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:HYN_8GB,SSD:256GB,WIFI:FCC
639-6667	PCBA,MLB,1.3GHZ,HY 8GB,TOSH 512G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:HYN_8GB,SSD:512GB,WIFI:FCC
639-6668	PCBA,MLB,1.3GHZ,SA 8GB,TOSH 256G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:SAM_8GB,SSD:256GB,WIFI:FCC
639-6669	PCBA,MLB,1.3GHZ,SA 8GB,TOSH 512G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:SAM_8GB,SSD:512GB,WIFI:FCC
639-6670	PCBA,MLB,1.1GHZ,HY 8GB,TOSH 128G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:HYN_8GB,SSD:128GB,WIFI:FCC
639-6671	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 256G,WIFI ETSI,X260	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,SSD:256GB,WIFI:ETSI
639-6672	PCBA,MLB,1.2GHZ,SA 8GB,TOSH 512G,WIFI APAC,X260	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:SAM_8GB,SSD:512GB,WIFI:APAC
639-6673	PCBA,MLB,1.2GHZ,EL 8GB,SAND 256G,WIFI ETSI,X260	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,SSD:256GB_SAND,WIFI:ETSI
639-6674	PCBA,MLB,1.3GHZ,EL 8GB,SAND 256G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,SSD:256GB_SAND,WIFI:FCC
639-6675	PCBA,MLB,1.3GHZ,SA 8GB,SAND 512G,WIFI APAC,X260	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:SAM_8GB,SSD:512GB_SAND,WIFI:APAC
639-6676	PCBA,MLB,1.2GHZ,EL 8GB,SAND 256G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,SSD:256GB_SAND,WIFI:FCC
639-6677	PCBA,MLB,1.3GHZ,SA 8GB,SAND 512G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:SAM_8GB,SSD:512GB_SAND,WIFI:FCC
639-6678	PCBA,MLB,1.3GHZ,HY 8GB,SAND 512G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:HYN_8GB,SSD:512GB_SAND,WIFI:FCC
639-6679	PCBA,MLB,1.2GHZ,HY 8GB,SAND 512G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:HYN_8GB,SSD:512GB_SAND,WIFI:FCC
639-6680	PCBA,MLB,1.1GHZ,HY 8GB,TOSH 512G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:HYN_8GB,SSD:512GB,WIFI:FCC
639-6681	PCBA,MLB,1.2GHZ,HY 8GB,TOSH 256G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:HYN_8GB,SSD:256GB,WIFI:FCC
639-6682	PCBA,MLB,1.2GHZ,SA 8GB,SAND 256G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:SAM_8GB,SSD:256GB_SAND,WIFI:FCC
639-6683	PCBA,MLB,1.3GHZ,SA 8GB,SAND 256G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:SAM_8GB,SSD:256GB_SAND,WIFI:FCC
639-6684	PCBA,MLB,1.1GHZ,SA 8GB,SAND 512G,WIFI ETSI,X260	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:SAM_8GB,SSD:512GB_SAND,WIFI:ETSI
639-6685	PCBA,MLB,1.2GHZ,SA 8GB,SAND 256G,WIFI IND,X260	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:SAM_8GB,SSD:256GB_SAND,WIFI:IND
639-6686	PCBA,MLB,1.3GHZ,HY 8GB,TOSH 128G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:HYN_8GB,SSD:128GB,WIFI:FCC
639-6687	PCBA,MLB,1.1GHZ,SA 8GB,TOSH 128G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:SAM_8GB,SSD:128GB,WIFI:FCC
639-6688	PCBA,MLB,1.1GHZ,HY 8GB,TOSH 256G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:HYN_8GB,SSD:256GB,WIFI:FCC
639-6689	PCBA,MLB,1.1GHZ,SA 8GB,SAND 256G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:SAM_8GB,SSD:256GB_SAND,WIFI:FCC
639-6690	PCBA,MLB,1.1GHZ,SA 8GB,SAND 512G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:SAM_8GB,SSD:512GB_SAND,WIFI:FCC
639-6691	PCBA,MLB,1.2GHZ,HY 8GB,TOSH 128G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:HYN_8GB,SSD:128GB,WIFI:FCC
639-6692	PCBA,MLB,1.2GHZ,SA 8GB,TOSH 128G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:SAM_8GB,SSD:128GB,WIFI:FCC
639-6693	PCBA,MLB,1.2GHZ,SA 8GB,TOSH 512G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:SAM_8GB,SSD:512GB,WIFI:FCC
639-6694	PCBA,MLB,1.3GHZ,SA 8GB,TOSH 128G,WIFI FCC,X260	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:SAM_8GB,SSD:128GB,WIFI:FCC

Partial & development BOMs

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00073	CMN PTS,PCBA,MLB,X260	MLB_COMMON
939-01879	PCBA,MLB,NO CPU,SA 8GB,TOSH 512G,WIFI FCC,X260	ALTERNATE,CMN,DRAM:SAM_8GB,SSD:512GB,WIFI:FCC
939-01880	PCBA,MLB,NO CPU,SA 8GB,SAND 512G,WIFI FCC,X260	ALTERNATE,CMN,DRAM:SAM_8GB,SSD:512GB_SAND,WIFI:FCC

BOM Groups

BOM GROUP	BOM OPTIONS
MLB_PROGPARTS	BOOTROM:PROG,BT:PROG,SMC:PROG,UPCROM:PROG

Common BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-00073	1	CMN PTS,PCBA,MLB,X260	CMNPTS	CRITICAL	CMN

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S00345	1	BT ROM (VXX) PROTO0,X260	U3770	CRITICAL	BT:PROG
341S00346	1	WIFI ROM (PXXXX) PROTO0,WW1,X260	U3780	CRITICAL	WIFI:FCC
341S00347	1	WIFI ROM (PXXXX) PROTO0,WW2,X260	U3780	CRITICAL	WIFI:ETSI
341S00348	1	WIFI ROM (PXXXX) PROTO0,WW3,X260	U3780	CRITICAL	WIFI:APAC
341S00349	1	WIFI ROM (PXXXX) PROTO0,IND,X260	U3780	CRITICAL	WIFI:IND

SYNC_MASTER=J43_MLB SYNC_DATE=10/24/2012

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X260 BOM Variants

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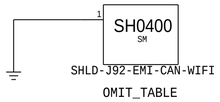
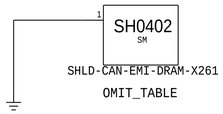
WIFI EMI CAN



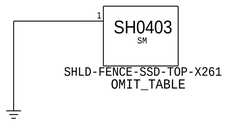
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-7064	1	CAN,EMI,WIFI,X261	SH0400	CRITICAL	

DRAM EMI CAN

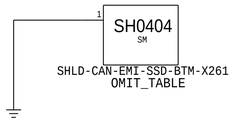


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-04848	1	CAN,EMI,DRAM,X260	SH0402	CRITICAL	

SSD EMI CANs

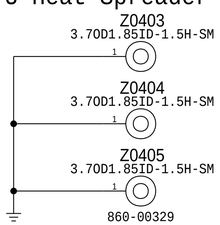


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-00889	1	FENCE,EMI,SSD,TOP,X261	SH0403	CRITICAL	
870-00878	1	TAPE,CONDUCTIVE,SSD,REEL,X261	SSD_TAPE_TOP	CRITICAL	

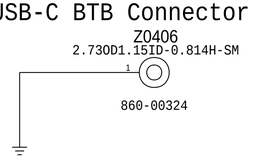


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-05622	1	FENCE,EMI,SSD,BTM,X260	SH0404	CRITICAL	
870-01557	1	TAPE,CONDUCTIVE,SSD,REEL,X260	SSD_TAPE_BTM	CRITICAL	

CPU Heat Spreader Bosses



USB-C BTB Connector Boss



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
870-00998	1	MYLAR,SHIM,MLB,X261	MYLAR_SHIM	CRITICAL	

SYNC_MASTER=J43_MLB SYNC_DATE=10/24/2012

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PD PARTS

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CRITICAL
OMIT_TABLE

DDI Port Assignments:

USBC Sink 0

USBC Sink 1

U0500
SKL-Y-ULX
BGA
SKL-Y
SYM 1 OF 20
DISPLAY

DDI

60 23	DP_XA_ML_C_N<0>	A46 DDI1_TXN0
60 23	DP_XA_ML_C_P<0>	C46 DDI1_TXP0
60 23	DP_XA_ML_C_N<1>	C48 DDI1_TXN1
60 23	DP_XA_ML_C_P<1>	A48 DDI1_TXP1
60 23	DP_XA_ML_C_N<2>	B45 DDI1_TXN2
60 23	DP_XA_ML_C_P<2>	D45 DDI1_TXP2
60 23	DP_XA_ML_C_N<3>	B47 DDI1_TXN3
60 23	DP_XA_ML_C_P<3>	D47 DDI1_TXP3
64	NC_DP_DDI2_ML_CN<0>	A42 DDI2_TXN0
64	NC_DP_DDI2_ML_CP<0>	C42 DDI2_TXP0
64	NC_DP_DDI2_ML_CN<1>	A44 DDI2_TXN1
64	NC_DP_DDI2_ML_CP<1>	C44 DDI2_TXP1
64	NC_DP_DDI2_ML_CN<2>	B41 DDI2_TXN2
64	NC_DP_DDI2_ML_CP<2>	D41 DDI2_TXP2
64	NC_DP_DDI2_ML_CN<3>	B43 DDI2_TXN3
64	NC_DP_DDI2_ML_CP<3>	D43 DDI2_TXP3

EDP

H45 EDP_TXN0	DP_INT_ML_C_N<0>	53
F45 EDP_TXP0	DP_INT_ML_C_P<0>	53
J44 EDP_TXN1	DP_INT_ML_C_N<1>	53
G44 EDP_TXP1	DP_INT_ML_C_P<1>	53
J46 EDP_TXN2	DP_INT_ML_C_N<2>	53
G46 EDP_TXP2	DP_INT_ML_C_P<2>	53
H43 EDP_TXN3	DP_INT_ML_C_N<3>	53
F43 EDP_TXP3	DP_INT_ML_C_P<3>	53
J42 EDP_AUXN	DP_INT_AUXCH_C_N	53
G42 EDP_AUXP	DP_INT_AUXCH_C_P	53
A40 EDP_DISP_UTIL	TP_EDP_DISP_UTIL	
H41 DDI1_AUXN	DP_XA_AUXCH_C_N	23 60
F41 DDI1_AUXP	DP_XA_AUXCH_C_P	23 60
J40 DDI2_AUXN	NC_DP_DDI2_AUXCH_CN	64
G40 DDI2_AUXP	NC_DP_DDI2_AUXCH_CP	64

eDP Port Assignment:

Internal panel

65 30 26 19 15 14 PLT_RST_L (IN)

61 47 11 8 PPVCCIO_S0
PLACE_NEAR=U0500.A50:15.24mm

R0520[1] 24.9 1% 1/20W MF 201 [2]

R0514[1] 100K 5% 1/32W MF 01005 [2]

59 (OUT)

DISPLAY SIDEBANDS

23 5 PCH_UPC_XA_SWD_CLK	L6	GPP_E18/DDPB_CTRLCLK
19 PCH_DDPB_CTRLDATA	H6	GPP_E19/DDPB_CTRLDATA (IPD-PLTRST#)
23 5 PCH_UPC_XA_SWD_DATA	H4	GPP_E20/DDPC_CTRLCLK
63 NC_PCH_DDPC_CTRLDATA	F4	GPP_E21/DDPC_CTRLDATA (IPD-PLTRST#)
SSD_RESET_L	M5	GPP_E22
64 5 TBT_POC_RESET	L4	GPP_E23 (IPD-PLTRST#)
MCP_EDP_RCOMP	A50	EDP_RCOMP

C11 GPP_E13/DDPB_HPD0	DP_DDI1_HPD	5 19
L10 GPP_E14/DDPC_HPD1	DP_DDI2_HPD	5 64
M7 GPP_E15/DDPD_HPD2	TP_PCH_GPP_E15	
F6 GPP_E16/DDPE_HPD3	JTAG_ISP_TDO	5 64
A7 GPP_E17/EDP_HPD	DP_INT_HPD	5 53
D4 EDP_BKLEN	EDP_BKLT_EN	5 52
B6 EDP_BKLCTL	EDP_BKLT_PWM	53 65
D3 EDP_VDDEN	EDP_PANEL_PWR	5 53

'Ridge systems: GPP_E18: JTAG_TBT_X_TMS
GPP_E20: JTAG_TBT_T_TMS

PP3V3_S0
6 14 15 16 17 19 23 26 27 31 33 34 35 39 46 50 51 53 61 67

R0510	10K	1 2					PCH_UPC_XA_SWD_CLK 5 23
R0512	10K	1 2	5%	1/32W	MF	01005	PCH_UPC_XA_SWD_DATA 5 23
R0515	100K	1 2	5%	1/32W	MF	01005	TBT_POC_RESET 5 64
R0580	100K	1 2	5%	1/32W	MF	01005	DP_DDI1_HPD 5 19
R0581	100K	1 2	5%	1/32W	MF	01005	DP_DDI2_HPD 5 64
R0583	10K	1 2	5%	1/32W	MF	01005	JTAG_ISP_TDO 5 64
R0584	100K	1 2	5%	1/32W	MF	01005	DP_INT_HPD 5 53
R0590	100K	1 2	5%	1/32W	MF	01005	EDP_BKLT_EN 5 52
R0591	100K	1 2	5%	1/32W	MF	01005	EDP_PANEL_PWR 5 53

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=DEVMLB SYNC_DATE=05/11/2015

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CPU GFX

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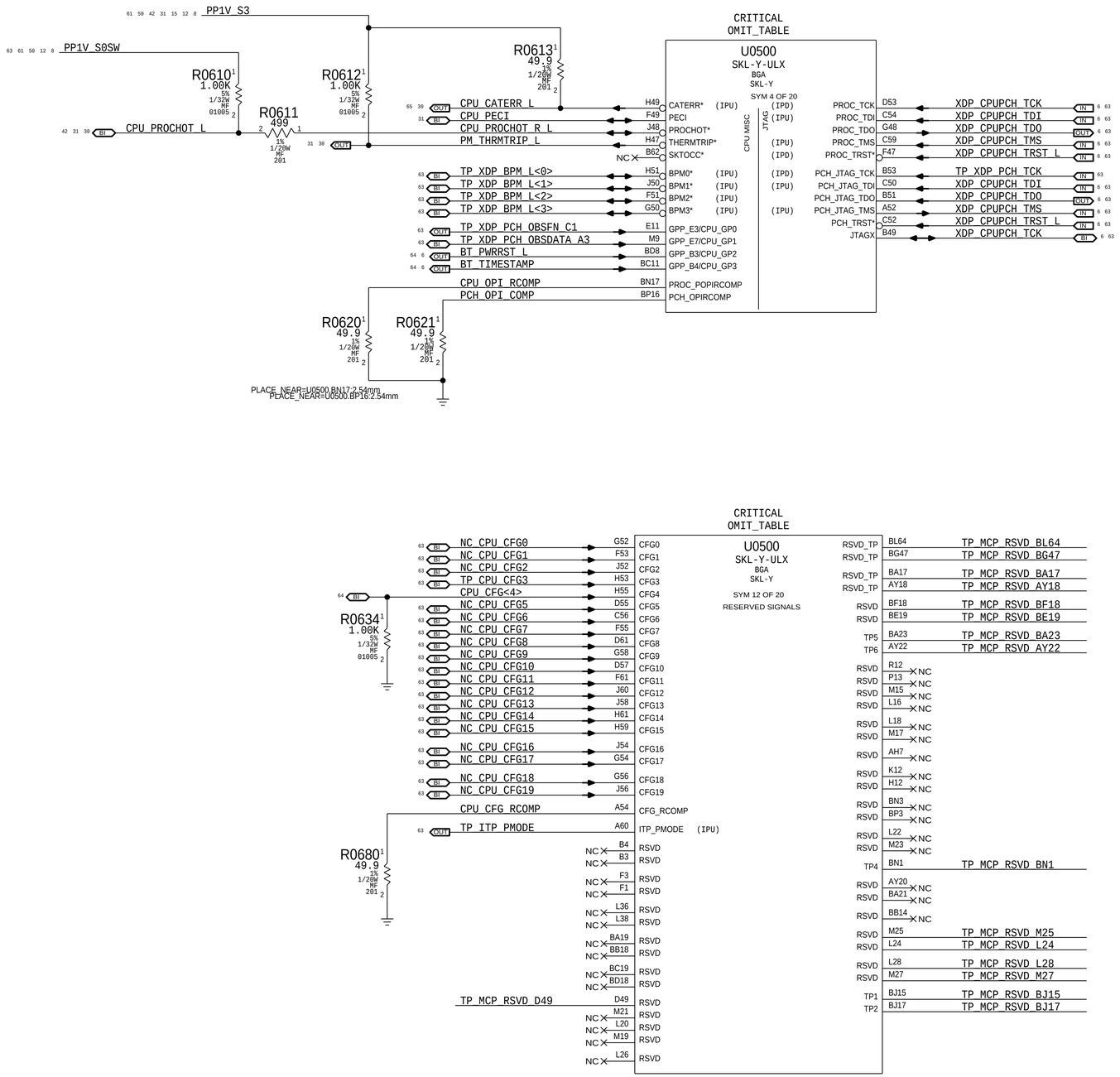

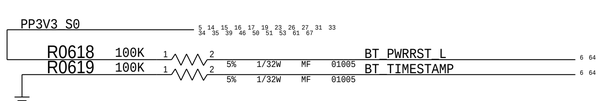

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=DEVMLB SYNC_DATE=05/11/2015

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CPU Misc/JTAG/CFG/RSVD

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CRITICAL
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U0500
SKL-Y-ULX
BGA
SKL-Y
SYM 2 OF 20
DDR CH - A

MEM_A_DQ<0>	AG61	DDR0_DQ0	
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MEM_A_DQ<9>	AM62	DDR0_DQ9	
MEM_A_DQ<10>	AT60	DDR0_DQ10	
MEM_A_DQ<11>	AR61	DDR0_DQ11	
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DDR1_DQSP1/DDR0_DQSP3	AJ55	MEM_A_DQS_P<3>
DDR0_DQSN2/DDR0_DQSN4	BD54	MEM_A_DQS_N<4>
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DDR0_DQSN3/DDR0_DQSN5	BF50	MEM_A_DQS_N<5>
DDR0_DQSP3/DDR0_DQSP5	BD50	MEM_A_DQS_P<5>
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DDR1_DQSP3/DDR0_DQSP7	BM50	MEM_A_DQS_P<7>
DDR0_ALERT*	BG57	
DDR0_PAR	BM56	NC
DDR_VREF_CA	AR53	CPU_DIMM_VREFCA
DDR0_VREF_DQ	AN53	CPU_DIMMA_VREFDQ
DDR1_VREF_DQ	AW53	CPU_DIMMB_VREFDQ
DDR_VTT_CNTL	BN47	TP_CPU_MEMVTT_PWR_EN

CRITICAL
OMIT_TABLE

U0500
SKL-Y-ULX
BGA
SKL-Y
SYM 3 OF 20
DDR CH - B

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MEM_B_DQ<5>	BD42	DDR0_DQ37/DDR1_DQ5	
MEM_B_DQ<6>	BG39	DDR0_DQ38/DDR1_DQ6	
MEM_B_DQ<7>	BE41	DDR0_DQ39/DDR1_DQ7	
MEM_B_DQ<8>	BC43	DDR0_DQ40/DDR1_DQ8	
MEM_B_DQ<9>	BD46	DDR0_DQ41/DDR1_DQ9	
MEM_B_DQ<10>	BG43	DDR0_DQ42/DDR1_DQ10	
MEM_B_DQ<11>	BG45	DDR0_DQ43/DDR1_DQ11	
MEM_B_DQ<12>	BC45	DDR0_DQ44/DDR1_DQ12	
MEM_B_DQ<13>	BE43	DDR0_DQ45/DDR1_DQ13	
MEM_B_DQ<14>	BE45	DDR0_DQ46/DDR1_DQ14	
MEM_B_DQ<15>	BF46	DDR0_DQ47/DDR1_DQ15	
MEM_B_DQ<16>	BM28	DDR1_DQ32/DDR1_DQ16	
MEM_B_DQ<17>	BN27	DDR1_DQ33/DDR1_DQ17	
MEM_B_DQ<18>	BK28	DDR1_DQ34/DDR1_DQ18	
MEM_B_DQ<19>	BL25	DDR1_DQ35/DDR1_DQ19	
MEM_B_DQ<20>	BN25	DDR1_DQ36/DDR1_DQ20	
MEM_B_DQ<21>	BL27	DDR1_DQ37/DDR1_DQ21	
MEM_B_DQ<22>	BJ25	DDR1_DQ38/DDR1_DQ22	
MEM_B_DQ<23>	BJ27	DDR1_DQ39/DDR1_DQ23	
MEM_B_DQ<24>	BM24	DDR1_DQ40/DDR1_DQ24	
MEM_B_DQ<25>	BK24	DDR1_DQ41/DDR1_DQ25	
MEM_B_DQ<26>	BN21	DDR1_DQ42/DDR1_DQ26	
MEM_B_DQ<27>	BJ23	DDR1_DQ43/DDR1_DQ27	
MEM_B_DQ<28>	BL23	DDR1_DQ44/DDR1_DQ28	
MEM_B_DQ<29>	BN23	DDR1_DQ45/DDR1_DQ29	
MEM_B_DQ<30>	BJ21	DDR1_DQ46/DDR1_DQ30	
MEM_B_DQ<31>	BL21	DDR1_DQ47/DDR1_DQ31	
MEM_B_DQ<32>	BN45	DDR0_DQ48/DDR1_DQ32	
MEM_B_DQ<33>	BM46	DDR0_DQ49/DDR1_DQ33	
MEM_B_DQ<34>	BL43	DDR0_DQ50/DDR1_DQ34	
MEM_B_DQ<35>	BK46	DDR0_DQ51/DDR1_DQ35	
MEM_B_DQ<36>	BN43	DDR0_DQ52/DDR1_DQ36	
MEM_B_DQ<37>	BL45	DDR0_DQ53/DDR1_DQ37	
MEM_B_DQ<38>	BJ45	DDR0_DQ54/DDR1_DQ38	
MEM_B_DQ<39>	BJ43	DDR0_DQ55/DDR1_DQ39	
MEM_B_DQ<40>	BM42	DDR0_DQ56/DDR1_DQ40	
MEM_B_DQ<41>	BN41	DDR0_DQ57/DDR1_DQ41	
MEM_B_DQ<42>	BJ41	DDR0_DQ58/DDR1_DQ42	
MEM_B_DQ<43>	BN39	DDR0_DQ59/DDR1_DQ43	
MEM_B_DQ<44>	BK42	DDR0_DQ60/DDR1_DQ44	
MEM_B_DQ<45>	BL41	DDR0_DQ61/DDR1_DQ45	
MEM_B_DQ<46>	BL39	DDR0_DQ62/DDR1_DQ46	
MEM_B_DQ<47>	BJ39	DDR0_DQ63/DDR1_DQ47	
MEM_B_DQ<48>	BF28	DDR1_DQ48	
MEM_B_DQ<49>	BD28	DDR1_DQ49	
MEM_B_DQ<50>	BG25	DDR1_DQ50	
MEM_B_DQ<51>	BC27	DDR1_DQ51	
MEM_B_DQ<52>	BG27	DDR1_DQ52	
MEM_B_DQ<53>	BE27	DDR1_DQ53	
MEM_B_DQ<54>	BE25	DDR1_DQ54	
MEM_B_DQ<55>	BC25	DDR1_DQ55	
MEM_B_DQ<56>	BF24	DDR1_DQ56	
MEM_B_DQ<57>	BD24	DDR1_DQ57	
MEM_B_DQ<58>	BG21	DDR1_DQ58	
MEM_B_DQ<59>	BC23	DDR1_DQ59	
MEM_B_DQ<60>	BE23	DDR1_DQ60	
MEM_B_DQ<61>	BG23	DDR1_DQ61	
MEM_B_DQ<62>	BC21	DDR1_DQ62	
MEM_B_DQ<63>	BE21	DDR1_DQ63	

DDR1_CKN0	BK36	MEM_B_CLK_N<0>
DDR1_CKP0	BM36	MEM_B_CLK_P<0>
DDR1_CKN1	BD32	MEM_B_CLK_N<1>
DDR1_CKP1	BF32	MEM_B_CLK_P<1>
DDR1_CKE0	BN33	MEM_B_CKE<0>
DDR1_CKE1	BK32	MEM_B_CKE<1>
DDR1_CKE2	BG33	MEM_B_CKE<2>
DDR1_CKE3	BH30	MEM_B_CKE<3>
DDR1_CS0*	BM30	MEM_B_CS_L<0>
DDR1_CS1*	BJ33	MEM_B_CS_L<1>
DDR1_ODT0	BC35	MEM_B_ODT<0>
DDR1_CAA0	BK30	MEM_B_CAA<0>
DDR1_CAA1	BN31	MEM_B_CAA<1>
DDR1_CAA2	BM32	MEM_B_CAA<2>
DDR1_CAA3	BL37	MEM_B_CAA<3>
DDR1_CAA4	BG31	MEM_B_CAA<4>
DDR1_CAA5	BN37	MEM_B_CAA<5>
DDR1_CAA6	BJ37	MEM_B_CAA<6>
DDR1_CAA7	BJ35	MEM_B_CAA<7>
DDR1_CAA8	BM34	MEM_B_CAA<8>
DDR1_CAA9	BN35	MEM_B_CAA<9>
DDR1_CAB0	BG37	MEM_B_CAB<0>
DDR1_CAB1	BE37	MEM_B_CAB<1>
DDR1_CAB2	BC37	MEM_B_CAB<2>
DDR1_CAB3	BF34	MEM_B_CAB<3>
DDR1_CAB4	BC33	MEM_B_CAB<4>
DDR1_CAB5	BF30	MEM_B_CAB<5>
DDR1_CAB6	BD36	MEM_B_CAB<6>
DDR1_CAB7	BG35	MEM_B_CAB<7>
DDR1_CAB8	BC31	MEM_B_CAB<8>
DDR1_CAB9	BF36	MEM_B_CAB<9>
DDR1_MA3	BJ31	NC
DDR1_MA4	BK34	NC
DDR0_DQSN4/DDR1_DQSN0	BD40	MEM_B_DQS_N<0>
DDR0_DQSP4/DDR1_DQSP0	BF40	MEM_B_DQS_P<0>
DDR0_DQSN5/DDR1_DQSN1	BD44	MEM_B_DQS_N<1>
DDR0_DQSP5/DDR1_DQSP1	BF44	MEM_B_DQS_P<1>
DDR1_DQSN4/DDR1_DQSN2	BK26	MEM_B_DQS_N<2>
DDR1_DQSP4/DDR1_DQSP2	BM26	MEM_B_DQS_P<2>
DDR1_DQSN5/DDR1_DQSN3	BM22	MEM_B_DQS_N<3>
DDR1_DQSP5/DDR1_DQSP3	BK22	MEM_B_DQS_P<3>
DDR0_DQSN6/DDR1_DQSN4	BK44	MEM_B_DQS_N<4>
DDR0_DQSP6/DDR1_DQSP4	BM44	MEM_B_DQS_P<4>
DDR0_DQSN7/DDR1_DQSN5	BM40	MEM_B_DQS_N<5>
DDR0_DQSP7/DDR1_DQSP5	BK40	MEM_B_DQS_P<5>
DDR1_DQSN6	BD26	MEM_B_DQS_N<6>
DDR1_DQSP6	BF26	MEM_B_DQS_P<6>
DDR1_DQSN7	BF22	MEM_B_DQS_N<7>
DDR1_DQSP7	BD22	MEM_B_DQS_P<7>
DDR1_ALERT*	BD34	
DDR1_PAR	BD30	NC
DRAM_RESET*	BP20	NC
DDR_RCOMP0	BF64	CPU_SM_RCOMP<0>
DDR_RCOMP1	BJ64	CPU_SM_RCOMP<1>
DDR_RCOMP2	BC64	CPU_SM_RCOMP<2>

R0752[1] 162 1% 1/20W MF 201 [2]
R0751[1] 80.6 1% 1/20W MF 201 [2]
R0750[1] 200 1% 1/20W MF 201 [2]

PLACE_NEAR=U0500.BC64:12.7mm
PLACE_NEAR=U0500.BJ64:12.7mm
PLACE_NEAR=U0500.BF64:12.7mm

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=DEVMLB SYNC_DATE=04/14/2015

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CPU LPDDR3 Interface

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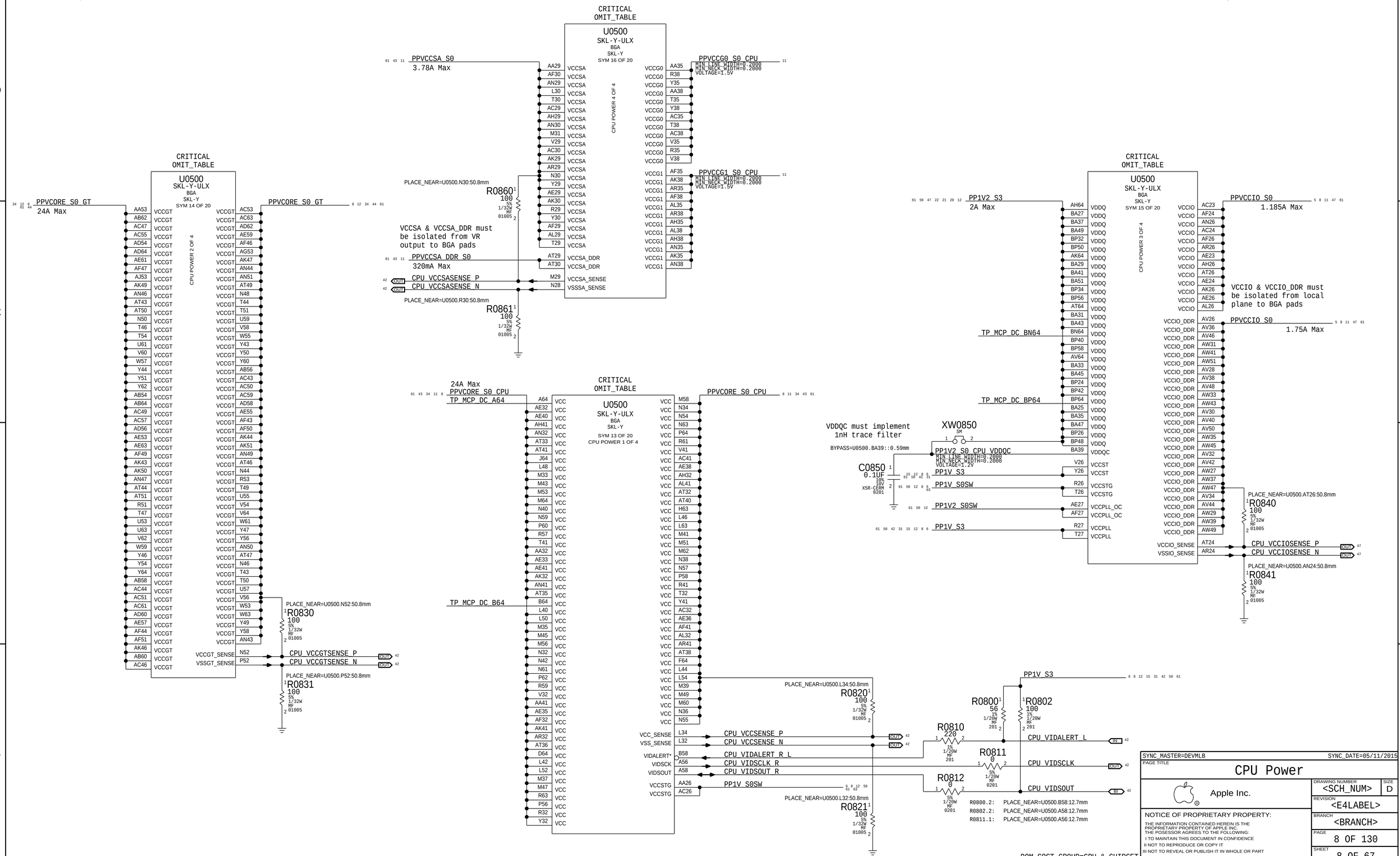
SKL-ULX current estimates from Skylake Processor EDS vol 1, doc #544924, v0.94
VCCIO breakdown per 4/20/15 email from Srini

NOTE: Aliases not used on CPU supply outputs to avoid any extraneous connections.



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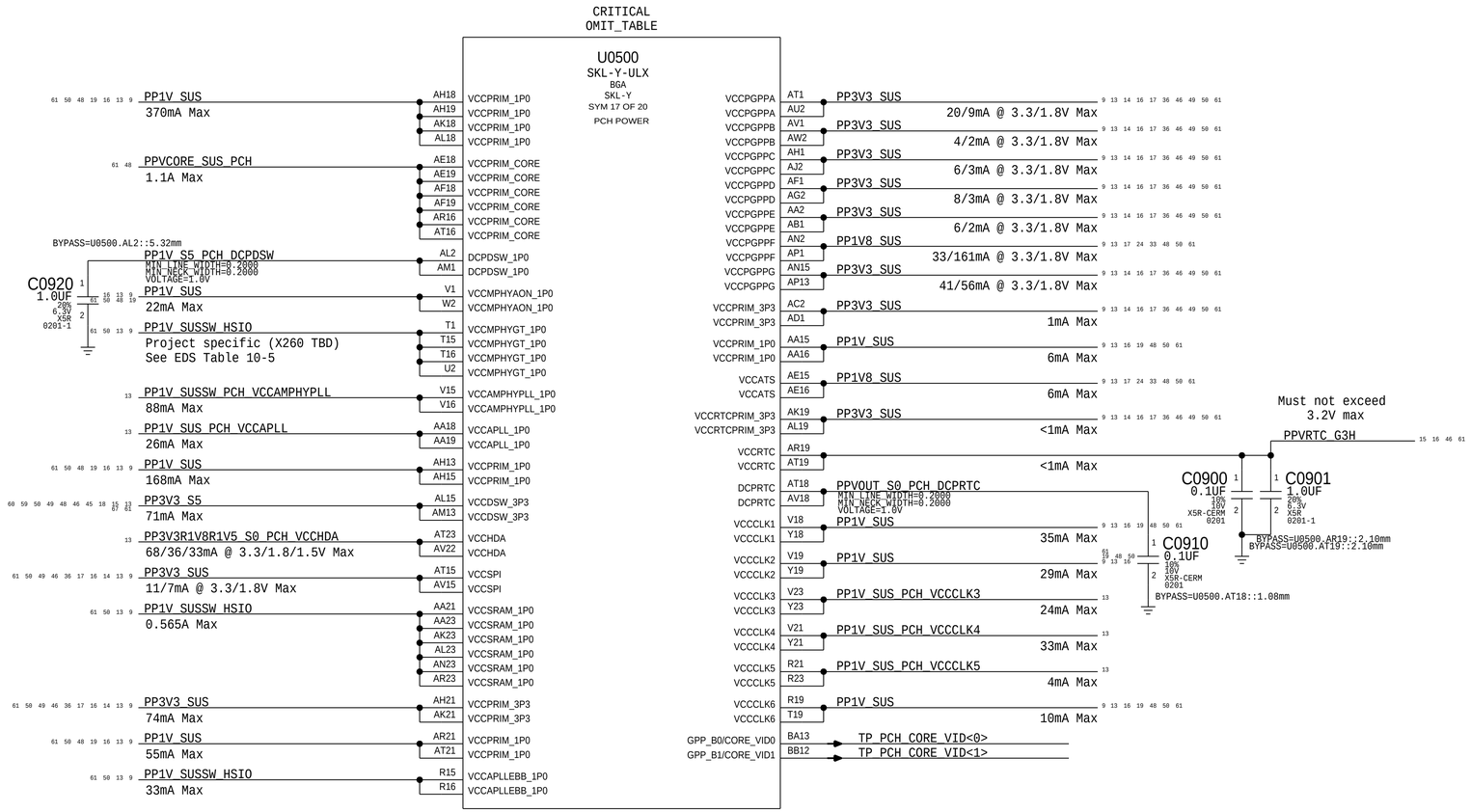
SPT-LP current estimates from Sunrise Point-LP PCH EDS vol 1, doc #545659, v1.2.
VCCAMPHYPLL_1P0 and VCCPRIM_1P0 / VCCPRIM_3P3 breakdowns from Srini email 4/13/15

NOTE: Aliases not used on CPU supply outputs to avoid any extraneous connections.



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PCH Power

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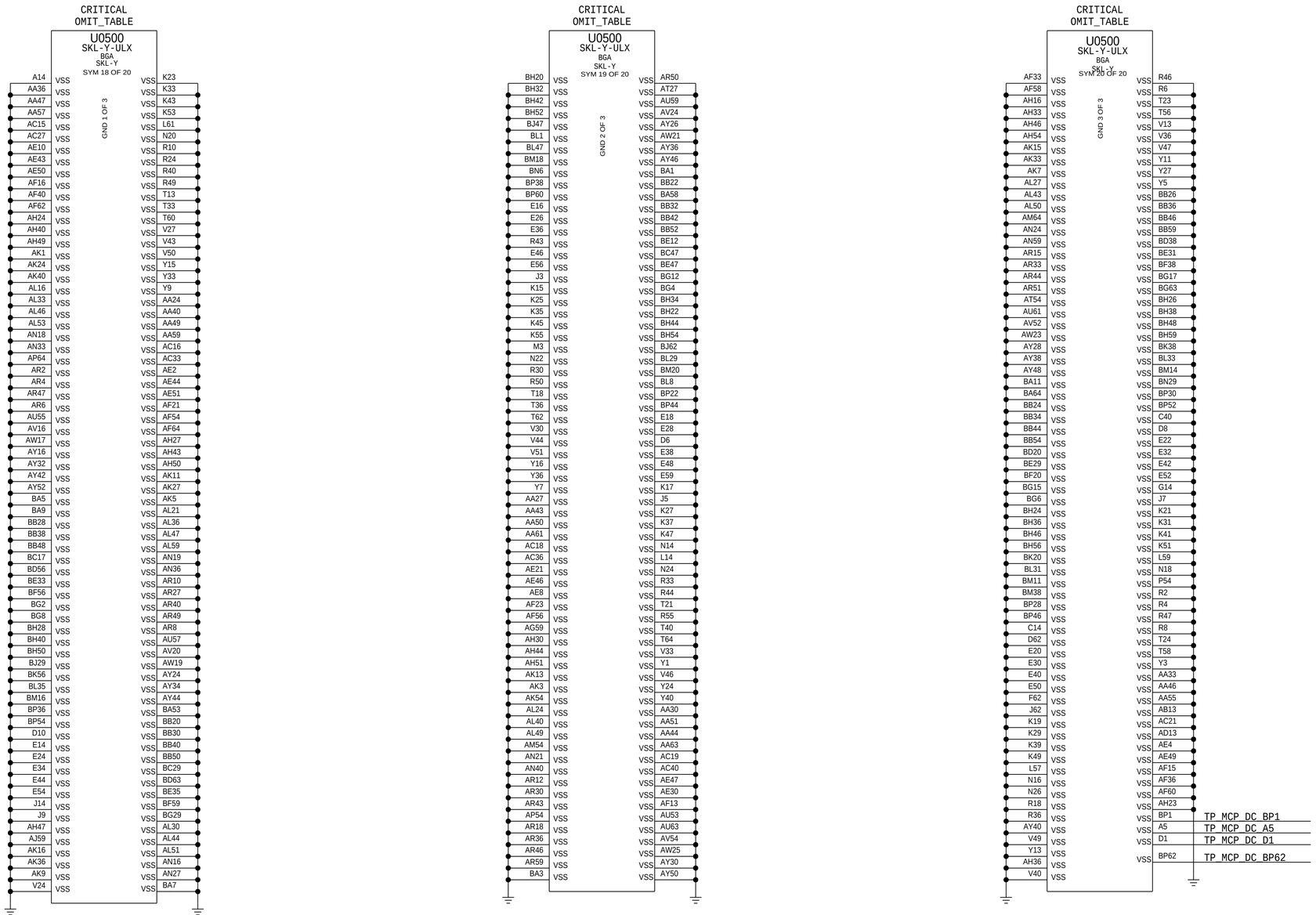

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CPU & PCH Grounds

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Intel's placeholders are no longer required per 4/20/15 email from Srini

CPU VCORE Decoupling

Intel recommendation (Table 52-2): 20x 0.1uF 0201 STUFF, 8x 10uF 0402, 6x 47uF 6.3V 0805 STUFF (2x NO STUFF)
Apple implementation : 20x 0.1uF 0201 STUFF (6x NO STUFF), 16x 20uF 0402, 3x 270uF 2V B2

61 43 34 8 PPVCORE_S0_CPU

C1100 0.1UF 10% 6.3V CERM-X5R 0201
C1101 0.1UF 10% 6.3V CERM-X5R 0201
C1102 0.1UF 10% 6.3V CERM-X5R 0201
C1103 0.1UF 10% 6.3V CERM-X5R 0201
C1104 0.1UF 10% 6.3V CERM-X5R 0201
C1105 0.1UF 10% 6.3V CERM-X5R 0201
C1106 0.1UF 10% 6.3V CERM-X5R 0201
C1107 0.1UF 10% 6.3V CERM-X5R 0201
C1108 0.1UF 10% 6.3V CERM-X5R 0201
C1109 0.1UF 10% 6.3V CERM-X5R 0201
C110A 0.1UF 10% 6.3V CERM-X5R 0201
C110B 0.1UF 10% 6.3V CERM-X5R 0201
C110C 0.1UF 10% 6.3V CERM-X5R 0201
C110D 0.1UF 10% 6.3V CERM-X5R 0201
C110E 0.1UF 10% 6.3V CERM-X5R 0201
C110F 0.1UF 10% 6.3V CERM-X5R 0201
C1110 0.1UF 10% 6.3V CERM-X5R 0201
C1111 0.1UF 10% 6.3V CERM-X5R 0201
C1112 0.1UF 10% 6.3V CERM-X5R 0201
C1113 0.1UF 10% 6.3V CERM-X5R 0201
NO STUFF C1114 0.1UF 10% 6.3V CERM-X5R 0201
NO STUFF C1115 0.1UF 10% 6.3V CERM-X5R 0201

NO STUFF C1116 0.1UF 10% 6.3V CERM-X5R 0201
NO STUFF C1117 0.1UF 10% 6.3V CERM-X5R 0201
NO STUFF C1118 0.1UF 10% 6.3V CERM-X5R 0201
NO STUFF C1119 0.1UF 10% 6.3V CERM-X5R 0201
C1132 12PF 5% 25V NPO-C0G 0201
C1133 12PF 5% 25V NPO-C0G 0201
CRITICAL C1120 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1121 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1122 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1123 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1124 20UF 20% 2.5V X6S-CERM 0402
NO STUFF C1125 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1126 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1127 20UF 20% 2.5V X6S-CERM 0402
NO STUFF C1128 20UF 20% 2.5V X6S-CERM 0402
NO STUFF C1129 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C112A 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C112B 20UF 20% 2.5V X6S-CERM 0402

CRITICAL C112C 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C112D 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C112E 20UF 20% 2.5V X6S-CERM 0402
NO STUFF C112F 20UF 20% 2.5V X6S-CERM 0402
OMIT_TABLE C1130 220UF 20% 2.0V POLY-TANT D1ST-D1L-COMBO
OMIT_TABLE C1131 220UF 20% 2.0V POLY-TANT D1ST-D1L-COMBO

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
128S00041	2	CAP,AL,POLY,220UF,20%,2V	C1130,C1131	CRITICAL	

CPU VCORE G0 Decoupling

Intel recommendation (Table 52-2): 12x 0.1uF 0201
Apple implementation : 12x 0.1uF 0201

8 PPVCCG0_S0_CPU

C1140 0.1UF 10% 6.3V CERM-X5R 0201
C1141 0.1UF 10% 6.3V CERM-X5R 0201
C1142 0.1UF 10% 6.3V CERM-X5R 0201
C1143 0.1UF 10% 6.3V CERM-X5R 0201
C1144 0.1UF 10% 6.3V CERM-X5R 0201
C1145 0.1UF 10% 6.3V CERM-X5R 0201
C1146 0.1UF 10% 6.3V CERM-X5R 0201
C1147 0.1UF 10% 6.3V CERM-X5R 0201
C1148 0.1UF 10% 6.3V CERM-X5R 0201
C1149 0.1UF 10% 6.3V CERM-X5R 0201
C114A 0.1UF 10% 6.3V CERM-X5R 0201
C114B 0.1UF 10% 6.3V CERM-X5R 0201

CPU VCORE G1 Decoupling

Intel recommendation (Table 52-2): 12x 0.1uF 0201
Apple implementation : 12x 0.1uF 0201

8 PPVCCG1_S0_CPU

C1150 0.1UF 10% 6.3V CERM-X5R 0201
C1151 0.1UF 10% 6.3V CERM-X5R 0201
C1152 0.1UF 10% 6.3V CERM-X5R 0201
C1153 0.1UF 10% 6.3V CERM-X5R 0201
C1154 0.1UF 10% 6.3V CERM-X5R 0201
C1155 0.1UF 10% 6.3V CERM-X5R 0201
C1156 0.1UF 10% 6.3V CERM-X5R 0201
C1157 0.1UF 10% 6.3V CERM-X5R 0201
C1158 0.1UF 10% 6.3V CERM-X5R 0201
C1159 0.1UF 10% 6.3V CERM-X5R 0201
C115A 0.1UF 10% 6.3V CERM-X5R 0201
C115B 0.1UF 10% 6.3V CERM-X5R 0201

CPU VCCIO Decoupling

Intel recommendation (Table 52-2): 13X 0.1UF 0201 STUFF (10x NO STUFF), 1x 1uF 0402, 1x 22uF 0805
Apple implementation : 13x 0.1uF 0201 STUFF (10x NO STUFF), 1x 1uF 0201, 1x 20uF 0402

61 47 8 5 PPVCCIO_S0

C1160 0.1UF 10% 6.3V CERM-X5R 0201
C1161 0.1UF 10% 6.3V CERM-X5R 0201
C1162 0.1UF 10% 6.3V CERM-X5R 0201
C1163 0.1UF 10% 6.3V CERM-X5R 0201
C1164 0.1UF 10% 6.3V CERM-X5R 0201
C1165 0.1UF 10% 6.3V CERM-X5R 0201
C1166 0.1UF 10% 6.3V CERM-X5R 0201
C1167 0.1UF 10% 6.3V CERM-X5R 0201
C1168 0.1UF 10% 6.3V CERM-X5R 0201
C1169 0.1UF 10% 6.3V CERM-X5R 0201
C116A 0.1UF 10% 6.3V CERM-X5R 0201
C116B 0.1UF 10% 6.3V CERM-X5R 0201
C116C 0.1UF 10% 6.3V CERM-X5R 0201
C1177 1.0UF 20% 6.3V X5R 0201-1
CRITICAL C1178 20UF 20% 2.5V X6S-CERM 0402

CPU VCCSA Decoupling

Intel recommendation (Table 52-2): 1x 1uF 0201, 4x 22uF 0603
Apple implementation : 1x 1uF 0201, 5x 0.1uF NO STUFF, 5x 20uF 0402, 1x 270uF 2V B2

61 43 8 PPVCCSA_S0

NO STUFF C1180 0.1UF 10% 6.3V CERM-X5R 0201
NO STUFF C1181 0.1UF 10% 6.3V CERM-X5R 0201
NO STUFF C1182 0.1UF 10% 6.3V CERM-X5R 0201
NO STUFF C1183 0.1UF 10% 6.3V CERM-X5R 0201
NO STUFF C1184 0.1UF 10% 6.3V CERM-X5R 0201
C118A 1.0UF 20% 6.3V X5R 0201-1
NO STUFF C118B 10UF 20% 4V X6S 0402
CRITICAL C118C 10UF 20% 4V X6S 0402
CRITICAL C118D 10UF 20% 4V X6S 0402
NO STUFF C118E 10UF 20% 4V X6S 0402
CRITICAL C118F 10UF 20% 4V X6S 0402
CRITICAL C1190 120UF 20% 2.5V TANT-POLY CASE-B2-SM

CPU VCCSA DDR Decoupling

Intel recommendation (Table 52-2): 1x 0.1uF 0201 STUFF, 1x 22uF 0603
Apple implementation : 1x 0.1uF 0201 STUFF, 1x 20uF 0402

61 43 8 PPVCCSA_DDR_S0

C1195 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL C1197 10UF 20% 4V X6S 0402

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SYNC_MASTER=DEVMLB SYNC_DATE=04/14/2015

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Intel's placeholders are no longer required per 4/20/15 email from Srini

CPU GT Decoupling

Intel recommendation (Table 52-2): 12x 0.1uF 0201 STUFF, 2x 1uF 0402, 2x 10uF 0402 NO STUFF, 9x 47uF 6.3V 0805
Apple implementation : 12x 0.1uF 0201 STUFF (20x NO STUFF), 2x 1uF 0201, 16x 20uF 0402, 2x 270uF 2V B2

61 44 34 8 PPVCORE_S0_GT

C1200 0.1UF 10% 6.3V CERM-X5R 0201	C1201 0.1UF 10% 6.3V CERM-X5R 0201	C1202 0.1UF 10% 6.3V CERM-X5R 0201	C1203 0.1UF 10% 6.3V CERM-X5R 0201	C1204 0.1UF 10% 6.3V CERM-X5R 0201	C1205 0.1UF 10% 6.3V CERM-X5R 0201	C1206 0.1UF 10% 6.3V CERM-X5R 0201	C1207 0.1UF 10% 6.3V CERM-X5R 0201	C1208 0.1UF 10% 6.3V CERM-X5R 0201	C1209 0.1UF 10% 6.3V CERM-X5R 0201	C1210 0.1UF 10% 6.3V CERM-X5R 0201	C1211 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1212 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1213 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1214 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1215 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1216 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1217 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1218 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1219 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1220 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1221 0.1UF 10% 6.3V CERM-X5R 0201

NO STUFF C1222 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1223 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1224 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1225 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1226 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1227 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1228 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1229 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1230 0.1UF 10% 6.3V CERM-X5R 0201	NO STUFF C1231 0.1UF 10% 6.3V CERM-X5R 0201

C1252 1.0UF 20% 6.3V X5R 0201-1	C1253 1.0UF 20% 6.3V X5R 0201-1	NO STUFF C1254 20UF 20% 2.5V X6S-CERM 0402	CRITICAL C1255 20UF 20% 2.5V X6S-CERM 0402	CRITICAL C1256 20UF 20% 2.5V X6S-CERM 0402	CRITICAL C1257 20UF 20% 2.5V X6S-CERM 0402	CRITICAL C1258 20UF 20% 2.5V X6S-CERM 0402	CRITICAL C1259 20UF 20% 2.5V X6S-CERM 0402	CRITICAL C125A 20UF 20% 2.5V X6S-CERM 0402	CRITICAL C125B 20UF 20% 2.5V X6S-CERM 0402	CRITICAL C125C 20UF 20% 2.5V X6S-CERM 0402	CRITICAL C125D 20UF 20% 2.5V X6S-CERM 0402	CRITICAL C125E 20UF 20% 2.5V X6S-CERM 0402	NO STUFF C125F 20UF 20% 2.5V X6S-CERM 0402

NO STUFF C1260 20UF 20% 2.5V X6S-CERM 0402	CRITICAL C1261 20UF 20% 2.5V X6S-CERM 0402	CRITICAL C1262 20UF 20% 2.5V X6S-CERM 0402	NO STUFF C1263 20UF 20% 2.5V X6S-CERM 0402	CRITICAL C1264 270UF 20% 2V 7.1MOHM CASE-B2-SM	CRITICAL C1265 270UF 20% 2V 7.1MOHM CASE-B2-SM

CPU VDDQ DECOUPLING

Intel recommendation (Table 52-2): 18x 0.1uF 0201
Apple implementation : 18x 0.1uF 0201

50 47 22 21 20 8 61 PP1V2_S3

C1270 0.1UF 10% 6.3V CERM-X5R 0201	C1271 0.1UF 10% 6.3V CERM-X5R 0201	C1272 0.1UF 10% 6.3V CERM-X5R 0201	C1273 0.1UF 10% 6.3V CERM-X5R 0201	C1274 0.1UF 10% 6.3V CERM-X5R 0201	C1275 0.1UF 10% 6.3V CERM-X5R 0201	C1276 0.1UF 10% 6.3V CERM-X5R 0201	C1277 0.1UF 10% 6.3V CERM-X5R 0201	C1278 0.1UF 10% 6.3V CERM-X5R 0201	C1279 0.1UF 10% 6.3V CERM-X5R 0201

C1280 0.1UF 10% 6.3V CERM-X5R 0201	C1281 0.1UF 10% 6.3V CERM-X5R 0201	C1282 0.1UF 10% 6.3V CERM-X5R 0201	C1283 0.1UF 10% 6.3V CERM-X5R 0201	C1284 0.1UF 10% 6.3V CERM-X5R 0201	C1285 0.1UF 10% 6.3V CERM-X5R 0201	C1286 0.1UF 10% 6.3V CERM-X5R 0201	C1287 0.1UF 10% 6.3V CERM-X5R 0201

CPU VCCST BYPASS
(CPU 1.0V SUSTAIN PWR)
42 31 15 12 8 6 61 50 PP1V_S3

C1290 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.V26::2.38mm

CPU VCCSTG BYPASS
(CPU 1.0V SUSTAIN GATED PWR)
63 61 50 8 6 PP1V_S0SW

C1292 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.R26::4.20mm

CPU VCCPLL_OC BYPASS
(CPU 1.2V PLL PWR)
61 50 8 PP1V2_S0SW

C1294 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.AE27::2.07mm

CPU VCCPLL BYPASS
(CPU 1.0V DIGITAL PLL PWR)
42 31 15 12 8 6 61 50 PP1V_S3

C1296 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.R27::1.99mm

NOTE: Bypass calcs based on 0.1mm trace width with worst case stackup and 500pH added for power/ground via pair.

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=DEVMLB SYNC_DATE=05/06/2015

PAGE TITLE: CPU Decoupling 2

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PCH VCCDSW_3P3 BYPASS
(PCH 3.3V DSW PWR)
PP3V3_S5
59 50 49 48 46 45 39 13 9 61 41 4a
C1300 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.AL15::1.96mm

PCH VCCATS BYPASS
(PCH 1.8V THERMAL PWR)
PP1V8_SUS
61 50 48 33 24 17 9
C1330 1.0UF 20% 6.3V X5R 0201-1
BYPASS=U0500.AE15::1.76mm

PCH VCCPRIM_1P0 BYPASS
(PCH 1.0V USB PWR)
PP1V_SUS
61 50 48 19 16 13 9
C1336 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.AH13::1.39mm

PCH VCCSPI BYPASS
(PCH 3.3V/1.8V SPI PWR)
PP3V3_SUS
50 49 46 36 17 16 14 13 9 61
C1302 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.AT15::2.38mm

PCH VCCMPHYAON_1P0 BYPASS
(PCH 1.0V MPHY ALWAYS ON PWR)
PP1V_SUS
61 50 48 19 16 13 9
C1340 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.V1::1.68mm

PCH VCCAPLLEBB BYPASS
(PCH 1.0V APLL EBB PWR)
PP1V_SUSSW_HSIO
61 50 13 9
C1344 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.R15::1.54mm

PCH VCCMPHYGT_1P0 BYPASS
(PCH 1.0V MPHY GATED PWR)
PP1V_SUSSW_HSIO
61 50 13 9
C1346 0.1UF 10% 6.3V X6S 0201
C1347 1.0UF 20% 6.3V X5R 0201-1
C1348 20UF 20% 6.3V CERM-X5R 0402
BYPASS=U0500.T15::3.07mm
BYPASS=U0500.T15::4.18mm
BYPASS=U0500.T15::4.18mm

PCH VCCRTCPRIM BYPASS
(PCH 3.3V SUSPEND RTC PWR)
PP3V3_SUS
50 49 46 36 17 16 14 13 9 61
C1306 1.0UF 20% 6.3V X5R 0201-1
C1307 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.AK19::1.68mm
BYPASS=U0500.AK19::1.68mm

PCH VCCAMPHYPLL_1P0 FILTER/BYPASS
(PCH 1.0V USB3/PCIE/SATA/MIPI PLL PWR)
PP1V_SUSSW_PCH_VCCAMPHYPLL
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=1.0V
61 50 13 9 PP1V_SUSSW_HSIO
R1370 0 5% 1/16W MF-LF 402
NOSTUFF C1370 20UF 20% 6.3V CERM-X5R 0402
NOSTUFF C1371 20UF 20% 6.3V CERM-X5R 0402
NOSTUFF C1372 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.V15::12.82mm
BYPASS=U0500.V15::12.82mm
BYPASS=U0500.V15::3.91mm

PCH VCCCLK3 FILTER/BYPASS
(PCH 1.0V CLOCK 3 PWR)
PP1V_SUS_PCH_VCCCLK3
MIN_LINE_WIDTH=0.0950
MIN_NECK_WIDTH=0.0700
VOLTAGE=1.0V
61 50 48 19 16 13 9 PP1V_SUS
R1380 0 5% 1/16W MF-LF 402
NOSTUFF C1380 20UF 20% 6.3V CERM-X5R 0402
NOSTUFF C1381 20UF 20% 6.3V CERM-X5R 0402
BYPASS=U0500.V19::10.17mm
BYPASS=U0500.V19::10.17mm

PCH VCCPGPPE BYPASS
(PCH 3.3V/1.8V GPIO GROUP E PWR)
PP3V3_SUS
61 50 49 46 36 17 16 14 13 9
C1318 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.AA2::0.84mm

PCH VCCCLK4 FILTER/BYPASS
(PCH 1.0V CLOCK 4 PWR)
PP1V_SUS_PCH_VCCCLK4
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=1.0V
19 16 13 9 61 50 4a PP1V_SUS
R1385 0 5% 1/16W MF-LF 402
NOSTUFF C1385 20UF 20% 6.3V CERM-X5R 0402
NOSTUFF C1386 20UF 20% 6.3V CERM-X5R 0402
BYPASS=U0500.V21::10.17mm
BYPASS=U0500.V21::10.17mm

PCH VCCCLK5 FILTER/BYPASS
(PCH 1.0V CLOCK 5 PWR)
PP1V_SUS_PCH_VCCCLK5
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=1.0V
61 50 48 19 16 13 9 PP1V_SUS
R1390 0 5% 1/16W MF-LF 402
NOSTUFF C1390 20UF 20% 6.3V CERM-X5R 0402
NOSTUFF C1391 20UF 20% 6.3V CERM-X5R 0402
C1392 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.R21::10.17mm
BYPASS=U0500.R21::10.17mm
BYPASS=U0500.R21::0.92mm

PCH VCCHDA FILTER/BYPASS
(PCH 3.3V/1.8V/1.5V HDA PWR)
PP3V3R1V8R1V5_S0_PCH_VCCHDA
MIN_LINE_WIDTH=0.0950
MIN_NECK_WIDTH=0.0700
VOLTAGE=1.5V
61 49 46 39 18 PP1V5_S0
L1309 220-OHM-0.7A-0.28-OHM 0402-1
C1309 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.AT23::1.23mm

PCH VCCAPLL FILTER/BYPASS
(PCH 1.0V APLL PWR)
PP1V_SUS_PCH_VCCAPLL
MIN_LINE_WIDTH=0.0950
MIN_NECK_WIDTH=0.0700
VOLTAGE=1.0V
61 50 48 19 16 13 9 PP1V_SUS
L1395 220-OHM-0.7A-0.28-OHM 0402-1
C1395 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.AA18::1.23mm

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=DEVMLB SYNC_DATE=05/11/2015

PAGE TITLE
PCH Decoupling

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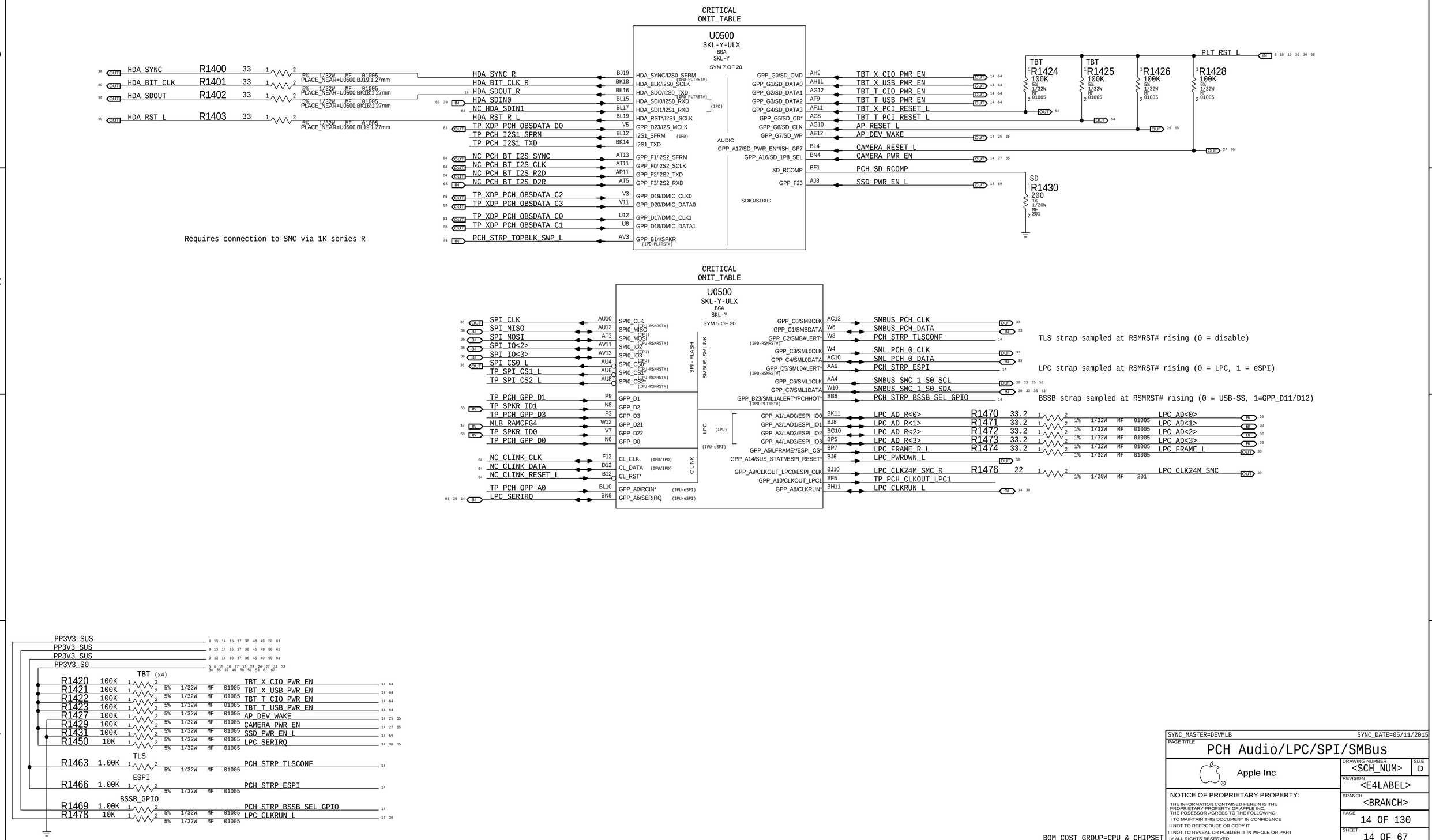

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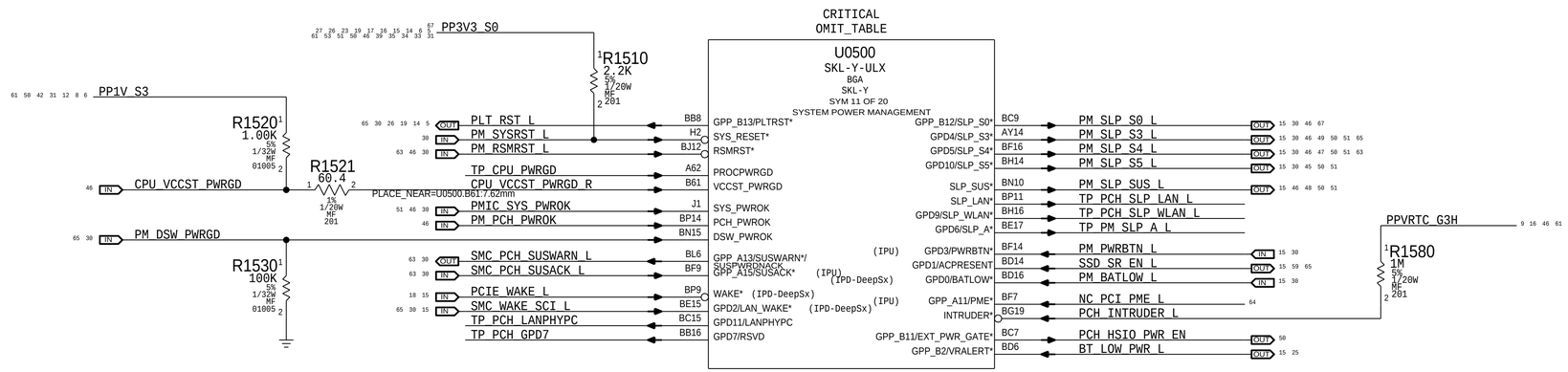

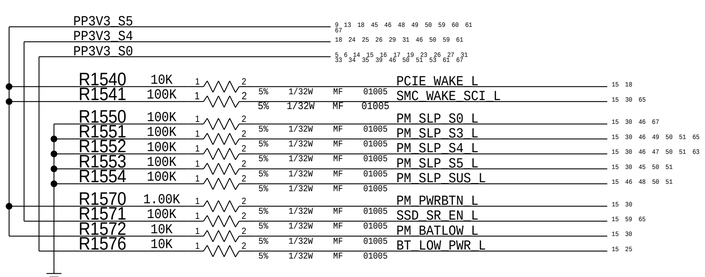

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SYNC_MASTER=X260_ERIC SYNC_DATE=06/04/2015

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PCH Power Management

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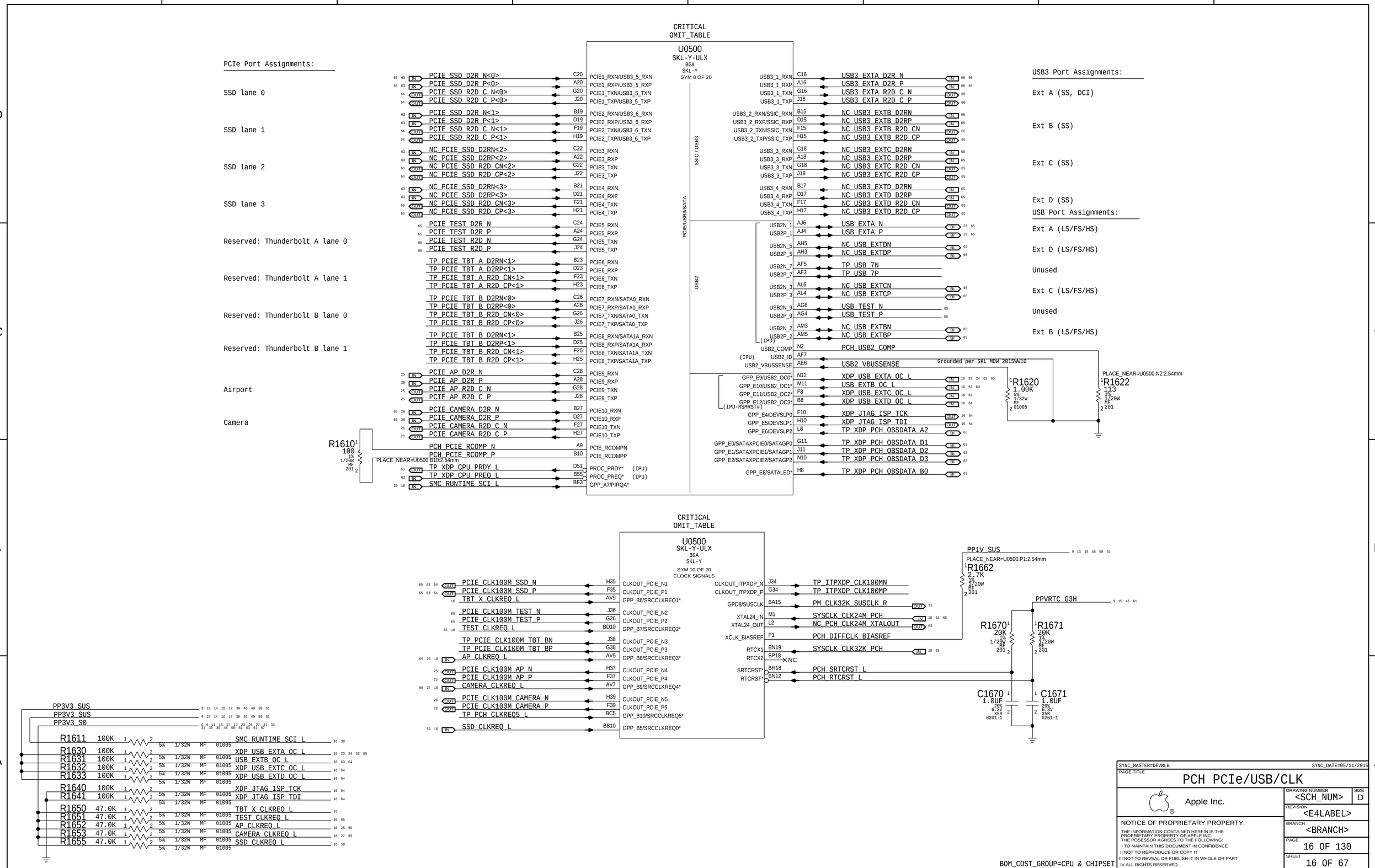

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CRITICAL
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U0500
SKL-Y-ULX
BGA
SKL-Y
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LPSS

AUD_SPI_CS_L	BC3	GPP_B15/GSPI0_CS*	
AUD_SPI_CLK	AW10	GPP_B16/GSPI0_CLK	
AUD_SPI_MISO	AW6	GPP_B17/GSPI0_MISO	
AUD_SPI_MOSI	BB4	GPP_B18/GSPI0_MOSI (IPD-PLTRST#)	
TPAD_SPI_CS_L	BB2	GPP_B19/GSPI1_CS*	
TPAD_SPI_CLK	AW12	GPP_B20/GSPI1_CLK	
TPAD_SPI_MISO	AW4	GPP_B21/GSPI1_MISO	
TPAD_SPI_MOSI	AW8	GPP_B22/GSPI1_MOSI (IPD-PLTRST#)	
PCH_BT_UART_D2R	AC8	GPP_C8/UART0_RXD	
PCH_BT_UART_R2D	AA8	GPP_C9/UART0_TXD	
PCH_BT_UART_RTS_L	AA10	GPP_C10/UART0_RTS*	
PCH_BT_UART_CTS_L	AA12	GPP_C11/UART0_CTS*	
SSD_UART_D2R	AD5	GPP_C20/UART2_RXD	
SSD_UART_R2D	AD7	GPP_C21/UART2_TXD	
LCD_PSR_EN	AD3	GPP_C22/UART2_RTS*	
SSD_UART_CTS_L	AD9	GPP_C23/UART2_CTS*	
AP_S0IX_WAKE_SEL	AD11	GPP_C16/I2C0_SDA	
AP_S0IX_WAKE_L	AB3	GPP_C17/I2C0_SCL	
TBT_X_PLUG_EVENT_L	AB9	GPP_C18/I2C1_SDA	
TBT_T_PLUG_EVENT_L	AB11	GPP_C19/I2C1_SCL	
I2C_UPC_SDA	AP3	GPP_F4/I2C2_SDA	
I2C_UPC_SCL	AP7	GPP_F5/I2C2_SCL	
UPC_I2C_INT_L	AP5	GPP_F6/I2C3_SDA	
SSD_BOOT_L	AT7	GPP_F7/I2C3_SCL	
TP_PCH_GPP_F8	AN4	GPP_F8/I2C4_SDA	
TP_PCH_GPP_F9	AN6	GPP_F9/I2C4_SCL	

ISH

P11	GPP_D9	MLB_BOARD_ID4
T7	GPP_D10	MLB_DEV_L
T5	GPP_D11	PCH_BSSB_CLK
T11	GPP_D12	PCH_BSSB_DATA
P7	GPP_D5/ISH_I2C0_SDA	MLB_BOARD_ID0
P5	GPP_D6/ISH_I2C0_SCL	MLB_BOARD_ID1
T9	GPP_D7/ISH_I2C1_SDA	MLB_BOARD_ID2
T3	GPP_D8/ISH_I2C1_SCL	MLB_BOARD_ID3
AM7	GPP_F10/I2C5_SDA/ISH_I2C2_SDA	TP_PCH_GPP_F10
AT9	GPP_F11/I2C5_SCL/ISH_I2C2_SCL	TP_PCH_GPP_F11
U10	GPP_D13/ISH_UART0_RXD/SML0BDATA	MLB_RAMCFG0
U4	GPP_D14/ISH_UART0_TXD/SML0BCLK	MLB_RAMCFG1
U6	GPP_D15/ISH_UART0_RTS*	MLB_RAMCFG2
V9	GPP_D16/ISH_UART0_CTS* /SML0BALERT*	MLB_RAMCFG3
AC6	GPP_C12/UART1_RXD/ISH_UART1_RXD	SOC_UART_D2R
AC4	GPP_C13/UART1_TXD/ISH_UART1_TXD	SOC_UART_R2D
AB7	GPP_C14/UART1_RTS*/ISH_UART1_RTS*	SOC_UART_RTS_L
AB5	GPP_C15/UART1_CTS*/ISH_UART1_CTS*	SOC_UART_CTS_L
BF11	GPP_A18/ISH_GP0	SPIROM_USE_MLB
BD2	GPP_A19/ISH_GP1	LCD_IRQ_L
BJ1	GPP_A20/ISH_GP2	TP_TBT_X_DPMUX_SEL
BL3	GPP_A21/ISH_GP3	TP_TBT_T_DPMUX_SEL
BJ3	GPP_A22/ISH_GP4	TPAD_SPI_IF_EN
BD4	GPP_A23/ISH_GP5	TPAD_SPI_INT_L
BJ4	SX_EXIT_HOLDOFF/GPP_A12 /BM_BUSY*/ISH_GP6	AUD_PWR_EN

CRITICAL
OMIT_TABLE

U0500
SKL-Y-ULX
BGA
SKL-Y
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CSI-2

NC	H29	CSI2_DN0	
NC	F29	CSI2_DP0	
NC	F33	CSI2_DN1	
NC	H33	CSI2_DP1	
NC	J30	CSI2_DN2	
NC	G30	CSI2_DP2	
NC	J32	CSI2_DN3	
NC	G32	CSI2_DP3	
NC	D29	CSI2_DN4	
NC	B29	CSI2_DP4	
NC	C32	CSI2_DN5	
NC	A32	CSI2_DP5	
NC	C30	CSI2_DN6	
NC	A30	CSI2_DP6	
NC	D33	CSI2_DN7	
NC	B33	CSI2_DP7	
NC	D35	CSI2_DN8	
NC	B35	CSI2_DP8	
NC	C36	CSI2_DN9	
NC	A36	CSI2_DP9	
NC	D37	CSI2_DN10	
NC	B37	CSI2_DP10	
NC	C38	CSI2_DN11	
NC	A38	CSI2_DP11	

CSI2_CLKN0	H31	NC
CSI2_CLKP0	F31	NC
CSI2_CLKN1	D31	NC
CSI2_CLKP1	B31	NC
CSI2_CLKN2	C34	NC
CSI2_CLKP2	A34	NC
CSI2_CLKN3	D39	NC
CSI2_CLKP3	B39	NC
CSI2_COMP	A11	PCH_CSI2_COMP
GPP_D4/FLASHTRIG	N4	TP_PCH_GPP_D4

CSI2
R1782 100 1% 1/20W MF 201

EMMC

GPP_F13/EMMC_DATA0	AN12	PCH_SWD_IO	OUT
GPP_F14/EMMC_DATA1	AP9	PCH_SWD_MUX_SEL	OUT
GPP_F15/EMMC_DATA2	AN10	SOC_WAKE_L	OUT
GPP_F16/EMMC_DATA3	AJ10	TP_PCH_GPP_F16	
GPP_F17/EMMC_DATA4	AM9	TP_PCH_GPP_F17	
GPP_F18/EMMC_DATA5	AL12	TP_PCH_GPP_F18	
GPP_F19/EMMC_DATA6	AJ12	TP_PCH_GPP_F19	
GPP_F20/EMMC_DATA7	AN8	TP_PCH_GPP_F20	
GPP_F21/EMMC_RCLK	AL10	TP_PCH_GPP_F21	
GPP_F22/EMMC_CLK	AL8	TP_PCH_GPP_F22	
GPP_F12/EMMC_CMD	AM11	PCH_SWD_CLK	OUT
EMMC_RCOMP	BC1	PCH_EMMC_RCOMP	

EMMC
R1795 200 1% 1/20W MF 201

PP3V3_S0
PP1V8_SUS

R1700	47.0K	5%	1/32W	MF	01005	AUD_SPI_CS_L	17	64
R1701	47.0K	5%	1/32W	MF	01005	AUD_SPI_CLK	17	64
R1702	47.0K	5%	1/32W	MF	01005	AUD_SPI_MISO	17	64
R1703	1.00K	5%	1/32W	MF	01005	AUD_SPI_MOSI	17	64
R1705	47.0K	5%	1/32W	MF	01005	TPAD_SPI_CS_L	17	29 65
R1706	47.0K	5%	1/32W	MF	01005	TPAD_SPI_CLK	17	29
R1707	47.0K	5%	1/32W	MF	01005	TPAD_SPI_MISO	17	29
R1708	150K	5%	1/20W	MF	201	TPAD_SPI_MOSI	17	29
R1710	47.0K	5%	1/32W	MF	01005	PCH_BT_UART_D2R	17	26 65
R1711	47.0K	5%	1/32W	MF	01005	PCH_BT_UART_R2D	17	26 65
R1712	47.0K	5%	1/32W	MF	01005	PCH_BT_UART_RTS_L	17	26 65
R1713	47.0K	5%	1/32W	MF	01005	PCH_BT_UART_CTS_L	17	26 65
R1715	47.0K	5%	1/32W	MF	01005	SSD_UART_D2R	17	63 65
R1716	47.0K	5%	1/32W	MF	01005	SSD_UART_R2D	17	63 65
R1717	100K	5%	1/32W	MF	01005	LCD_PSR_EN	17	64
R1718	47.0K	5%	1/32W	MF	01005	SSD_UART_CTS_L	17	
R1720	100K	5%	1/32W	MF	01005	AP_S0IX_WAKE_SEL	17	18 65
R1721	100K	5%	1/32W	MF	01005	AP_S0IX_WAKE_L	17	18 65
R1722	100K	5%	1/32W	MF	01005	TBT_X_PLUG_EVENT_L	17	64
R1723	100K	5%	1/32W	MF	01005	TBT_T_PLUG_EVENT_L	17	64
R1727	100K	5%	1/32W	MF	01005	SSD_BOOT_L	17	54 65

PP3V3_SUS
PP1V8_SUS
PP3V3_S0

MLB_DEV

MLB_DEV_L	R1750	1.00K	5%	1/32W	MF	01005	17	
SOC_UART_D2R	R1770	47.0K	5%	1/32W	MF	01005	64	17
SOC_UART_R2D	R1771	47.0K	5%	1/32W	MF	01005	64	17
SOC_UART_RTS_L	R1772	47.0K	5%	1/32W	MF	01005	64	17
SOC_UART_CTS_L	R1773	47.0K	5%	1/32W	MF	01005	64	17
SPIROM_USE_MLB	R1774	100K	5%	1/32W	MF	01005	36	17
LCD_IRQ_L	R1775	100K	5%	1/32W	MF	01005	65 53	17
TPAD_SPI_IF_EN	R1778	100K	5%	1/32W	MF	01005	65 29	17
TPAD_SPI_INT_L	R1779	100K	5%	1/32W	MF	01005	65 29	17
AUD_PWR_EN	R1780	100K	5%	1/32W	MF	01005	65 39	17
PCH_SWD_IO	R1784	100K	5%	1/32W	MF	01005	64	17
PCH_SWD_MUX_SEL	R1785	100K	5%	1/32W	MF	01005	64	17
SOC_WAKE_L	R1786	100K	5%	1/32W	MF	01005	64	17
PCH_SWD_CLK	R1794	100K	5%	1/32W	MF	01005	64	17

Board ID Straps

MLB_BOARD_ID0
MLB_BOARD_ID1
MLB_BOARD_ID2
MLB_BOARD_ID3
MLB_BOARD_ID4

BOARDID4_L	BOARDID3_L	BOARDID2_L	BOARDID1_L	BOARDID0_L
R1759	R1758	R1757	R1756	R1755
1.00K 5% 1/32W MF 01005	1.00K 5% 1/32W MF 01005	1.00K 5% 1/32W MF 01005	1.00K 5% 1/32W MF 01005	1.00K 5% 1/32W MF 01005

RAM Configuration Straps

MLB_RAMCFG0
MLB_RAMCFG1
MLB_RAMCFG2
MLB_RAMCFG3
MLB_RAMCFG4

RAMCFG4_L	RAMCFG3_L	RAMCFG2_L	RAMCFG1_L	RAMCFG0_L
R1769	R1768	R1767	R1766	R1765
1.00K 5% 1/32W MF 01005	1.00K 5% 1/32W MF 01005	1.00K 5% 1/32W MF 01005	1.00K 5% 1/32W MF 01005	1.00K 5% 1/32W MF 01005

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=DEVMLB SYNC_DATE=05/11/2015

PAGE TITLE
PCH GPIO/LPSS

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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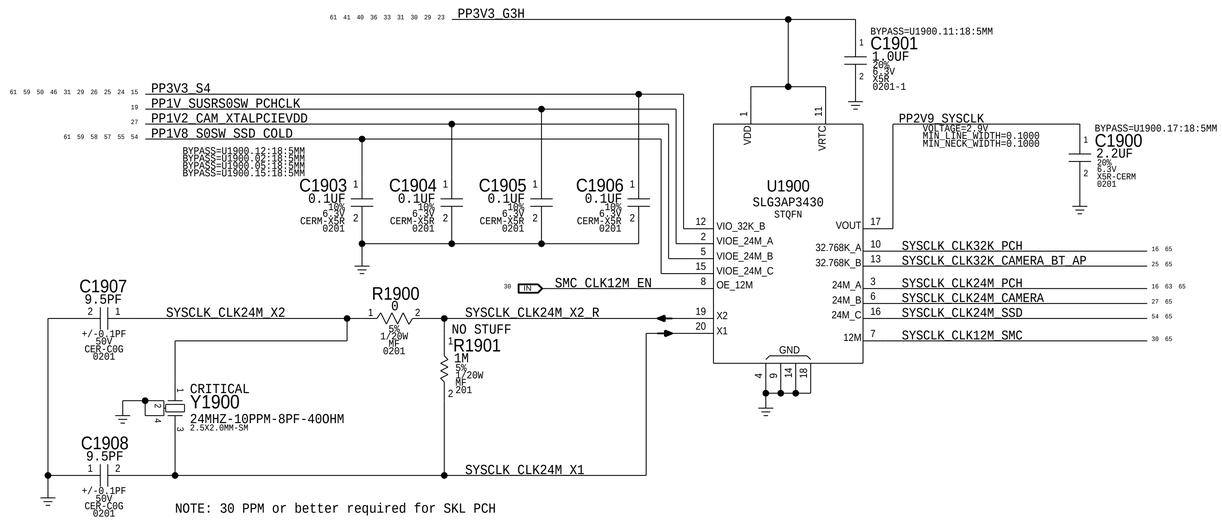
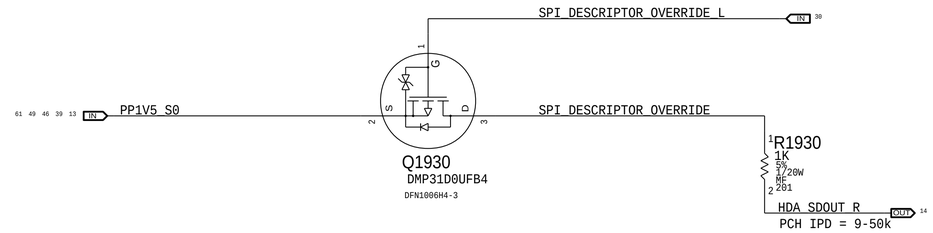
System 32kHz / 12MHz / 24MHz Clock Generator



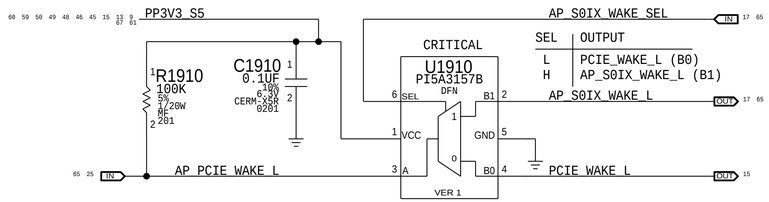
NOTE: 30 PPM or better required for SKL PCH

PCH ME Disable Strap



PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
***** Circuit does not support HDA voltage >3.3V.

PCIe Wake Muxing



BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE	Chipset Support 1
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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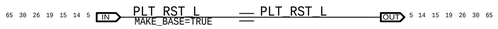
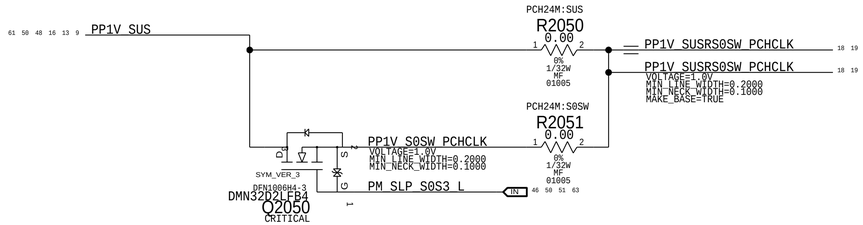
Platform Reset Connections

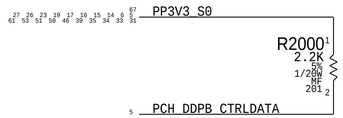
Unbuffered



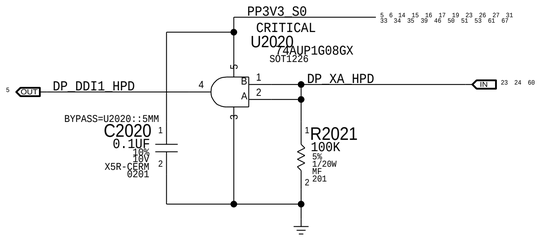
PCH 24MHz VIOE Options



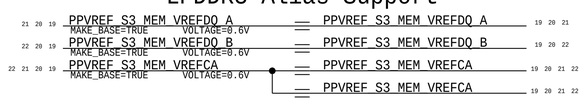
DP DDP Straps



HPD S0 Isolation



LPDDR3 Alias Support



SYNC_MASTER=X260_ERIC SYNC_DATE=06/09/2015

PAGE TITLE

Project Chipset Support

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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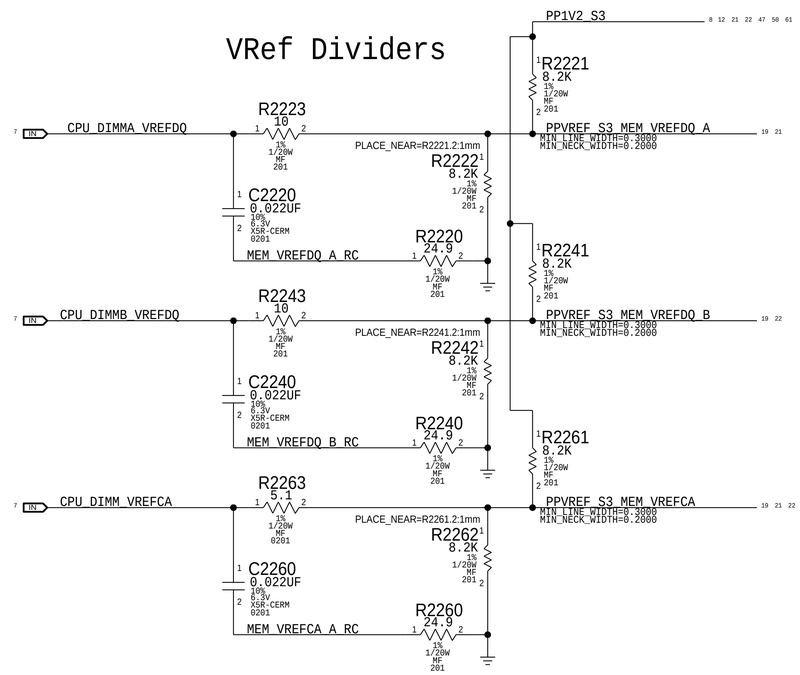
CPU-Based Margining

VRef Dividers



SYNC_MASTER=DEVMLB SYNC_DATE=04/14/2015

PAGE TITLE
LPDDR3 VREF MARGINING

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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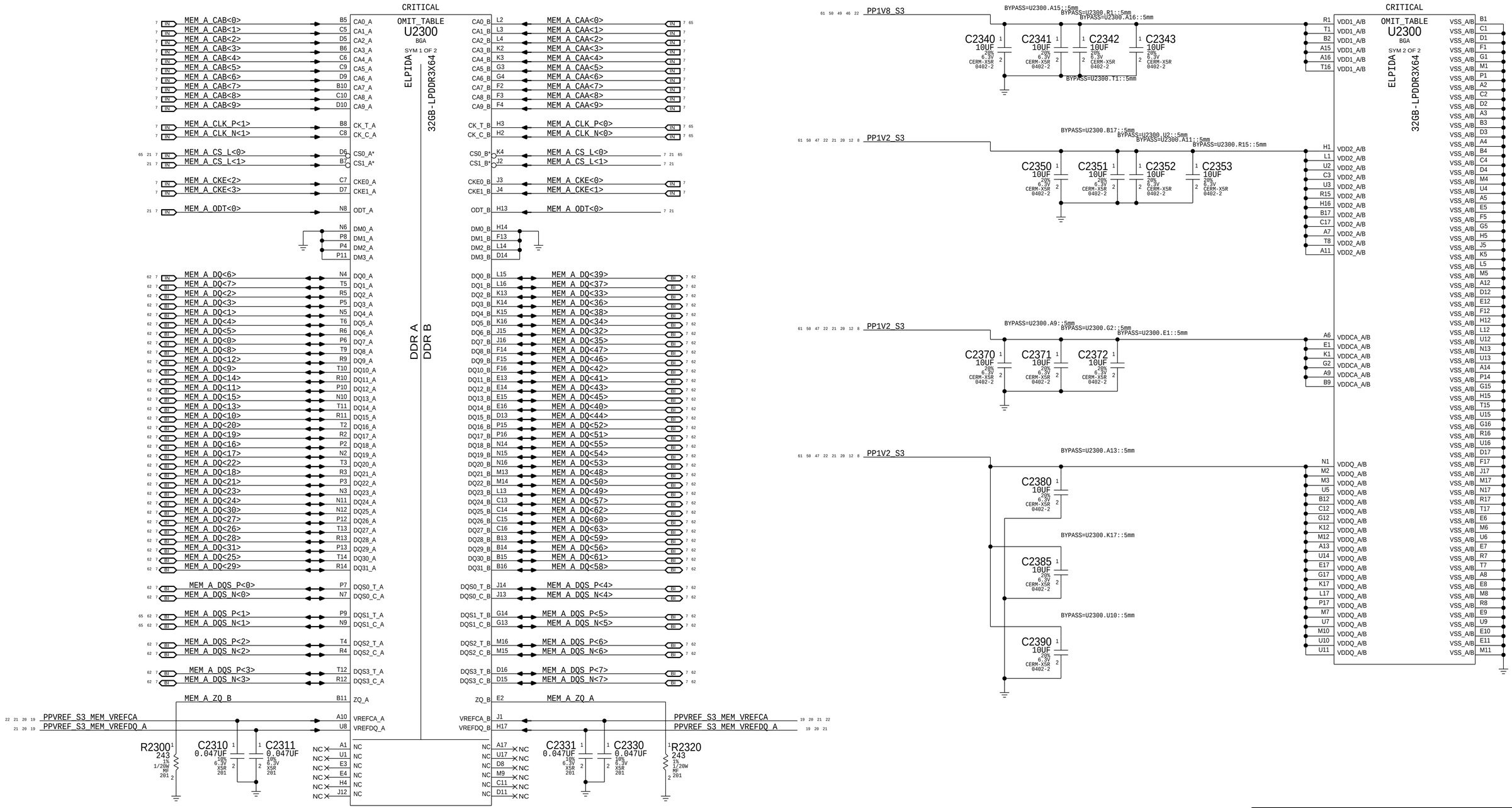

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PAGE TITLE

LPDDR3 DRAM Channel A (0-63)

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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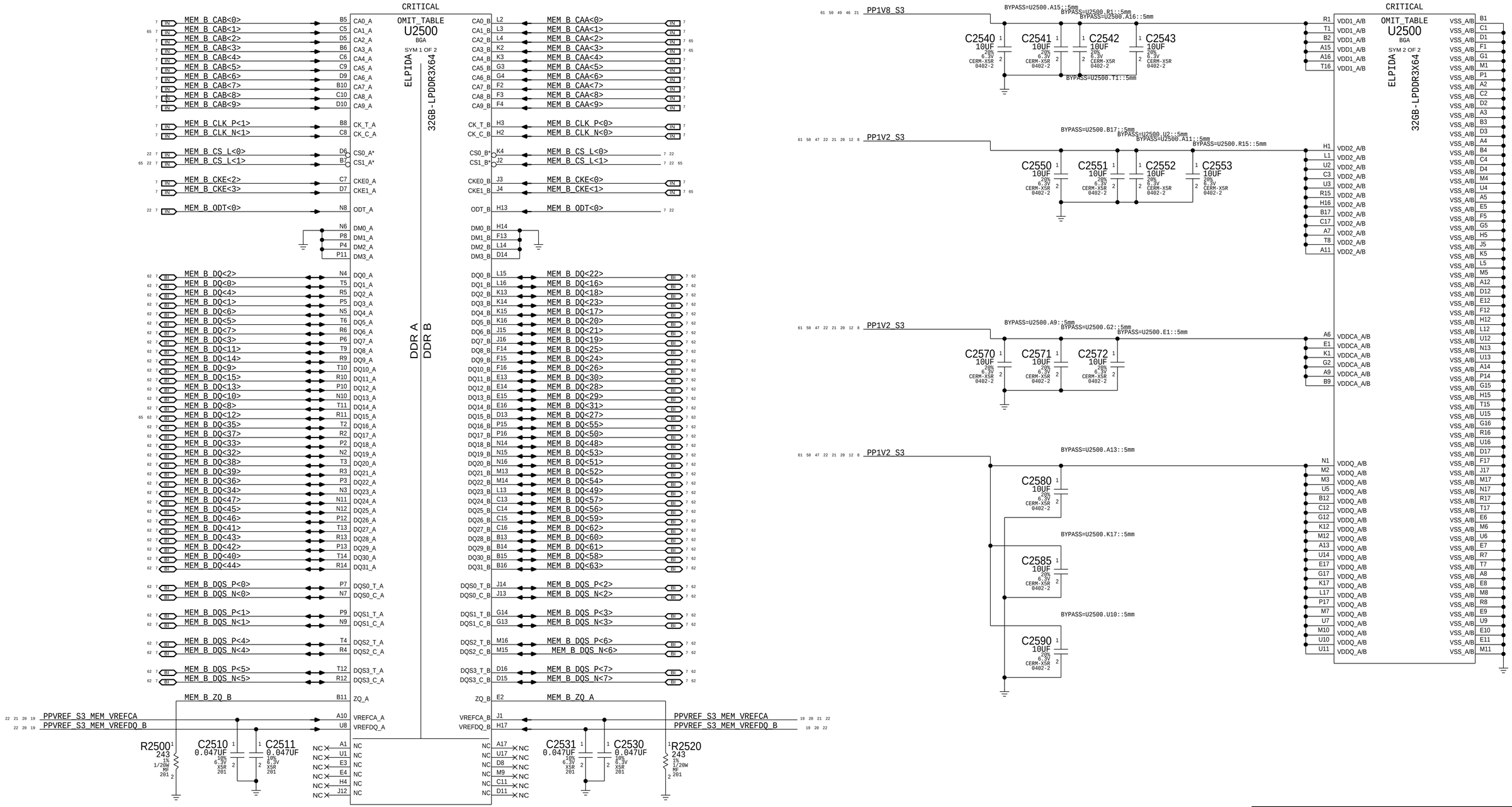

SYNC_MASTER=DEVMLB SYNC_DATE=04/14/2015

PAGE TITLE
LPDDR3 DRAM Channel B (0-63)

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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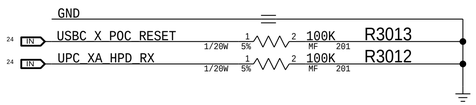
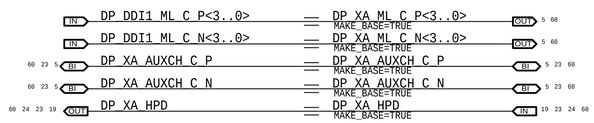
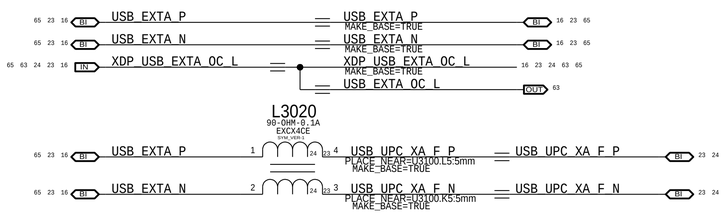
'Ridge-less Support



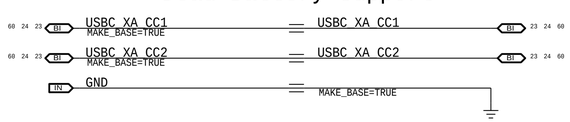
DP Support



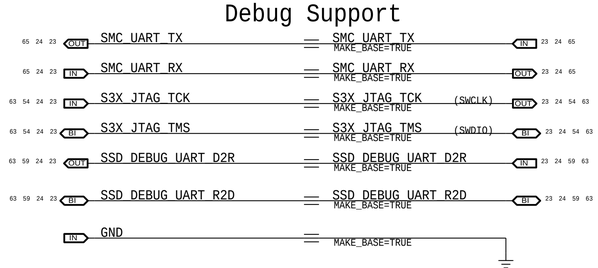
USB Support

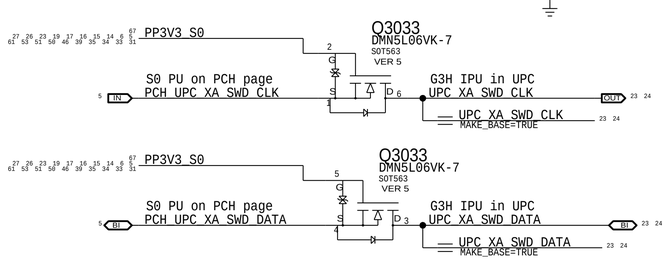


Dead Battery Support

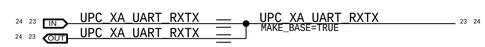


Debug Support





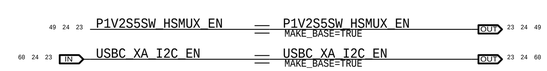
Single Port Support



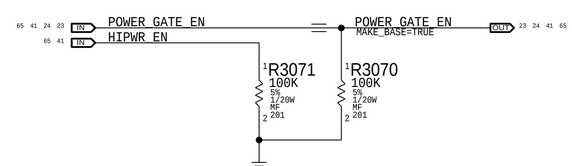
Bring Up Support

VIN_3V3 power currently required to drive POWER_GATE_EN high. Future OTP update may enable usage of 3V3_G3H instead.

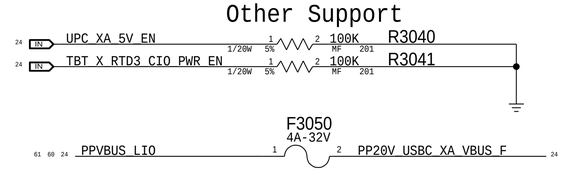
High Speed Mux Support



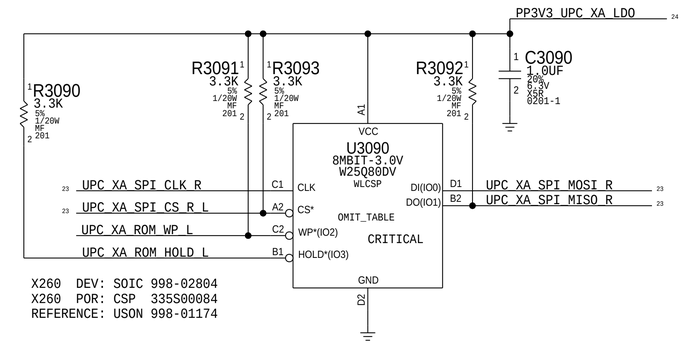
Bansuri Support



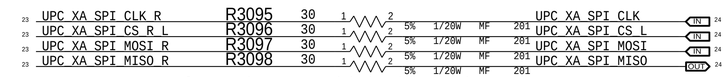
Other Support



Port Controller ROM



X260 DEV: SOIC 998-02804
X260 POR: CSP 335S00084
REFERENCE: USON 998-01174



Place series R at T with dev debug header
Characterize series R on P0 Dev, hopefully remove for P0 POR

SYNC_MASTER=X260_ERIC SYNC_DATE=06/04/2019

PAGE TITLE
USB-C Port Controller Support

Apple Inc.

DRAWING NUMBER	<SCH_NUM>
SIZE	D
REVISION	<E4LABEL>
BRANCH	<BRANCH>
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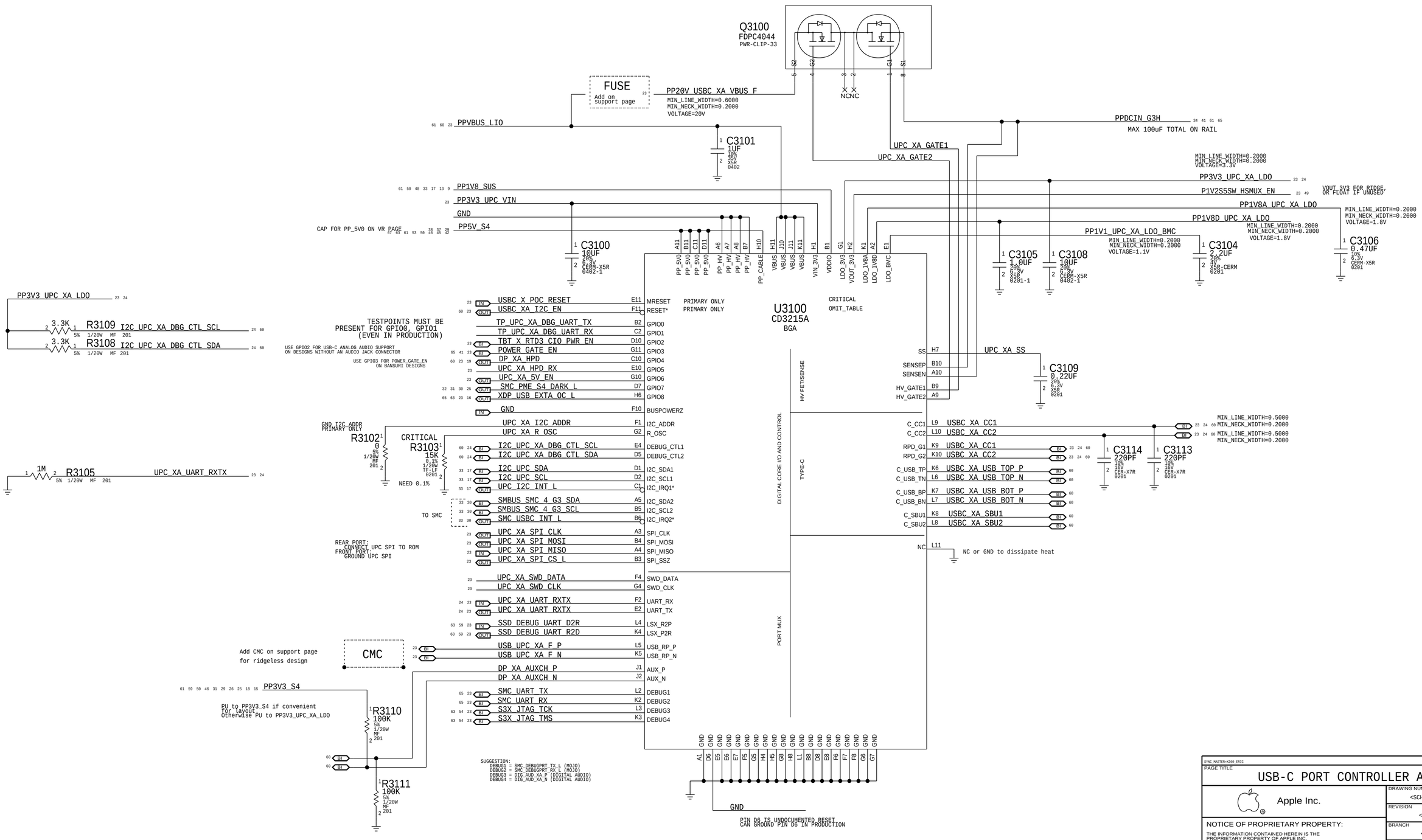
PRIMARY ACE USB-C PORT CONTROLLER (UPC)



BOM_COST_GROUP=USB-C

PAGE TITLE: USB-C PORT CONTROLLER A

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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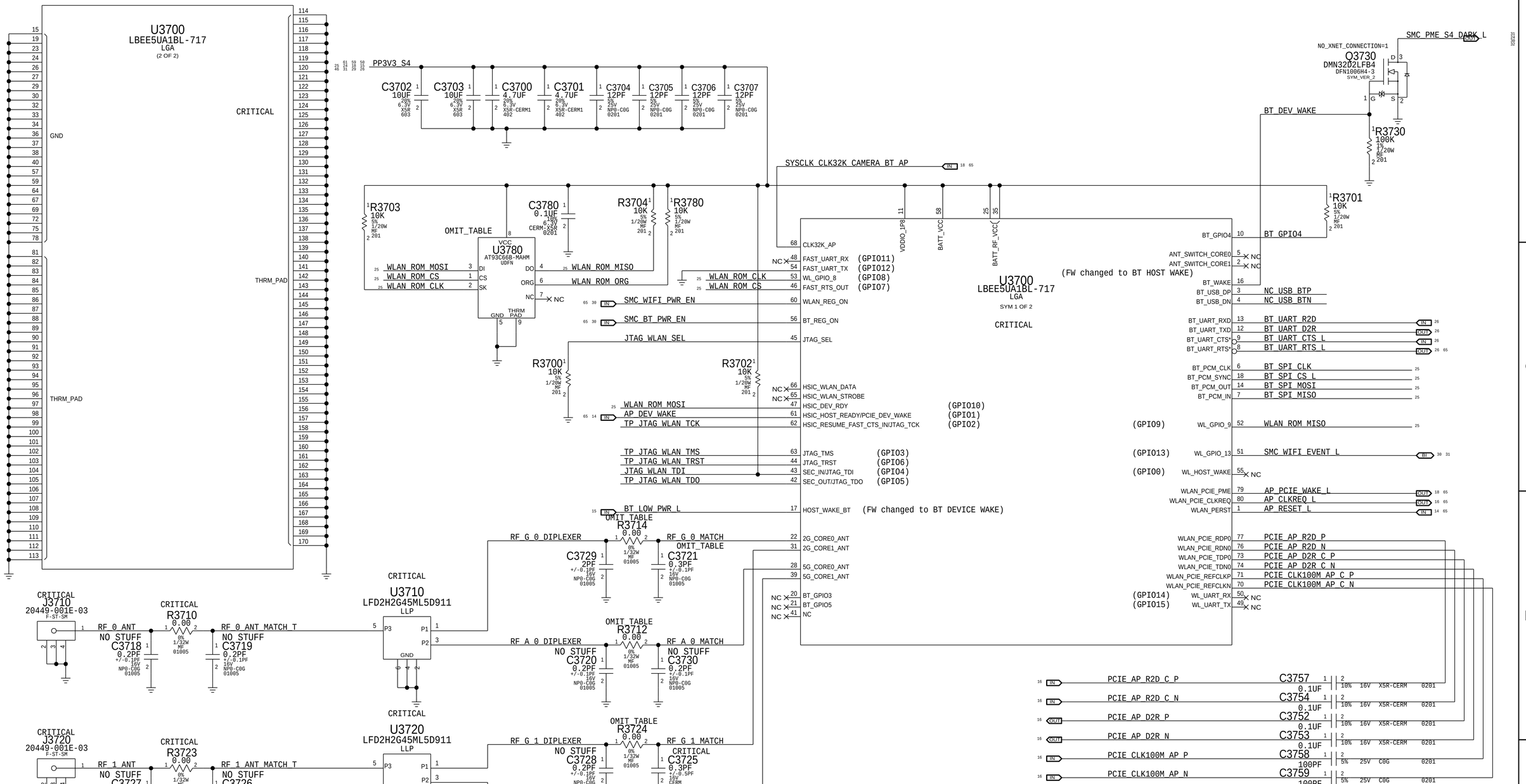

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
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152S1742	1	IND,FILM,1.6NH,+/-0.1NH,200MA,01005	C3721	CRITICAL	
152S1544	1	IND,FILM,0.4NH,+/-0.1NH,270MA,01005	R3712	CRITICAL	
152S1564	1	IND,FILM,2.4NH,+/-0.1NH,200MA,01005	R3724	CRITICAL	
152S1720	1	IND,FILM,1.8NH,+/-0.1NH,270MA,01005	C3724	CRITICAL	

SYNC_MASTER=DEVMLB SYNC_DATE=07/20/2015

PAGE TITLE
WIFI/BT MODULE [37]

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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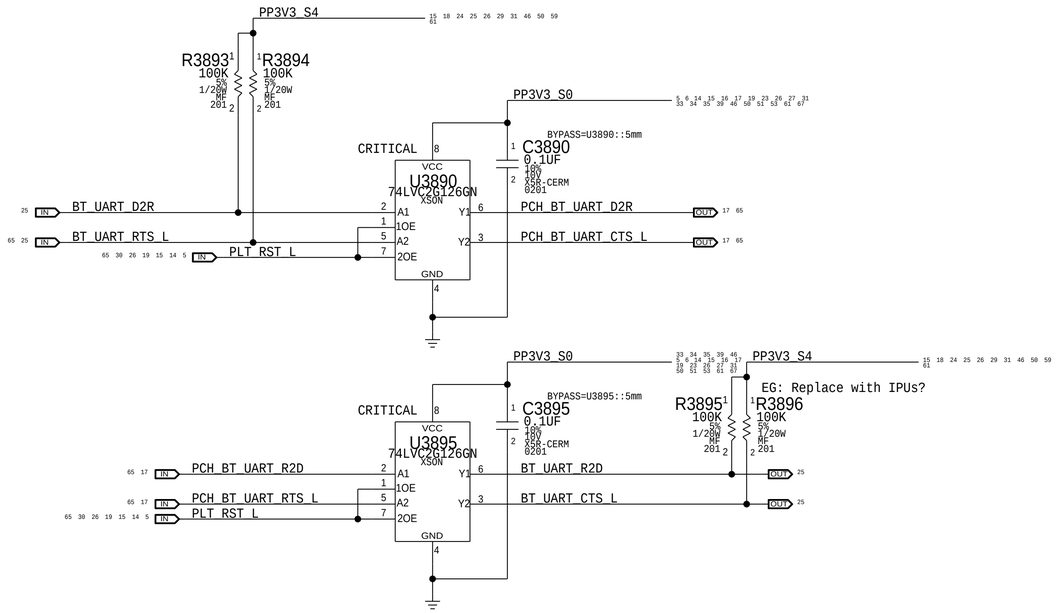
BT UART Isolation



SYNC_MASTER=J92_DEVMLB SYNC_DATE=05/13/2015

PAGE TITLE

WIFI/BT Support

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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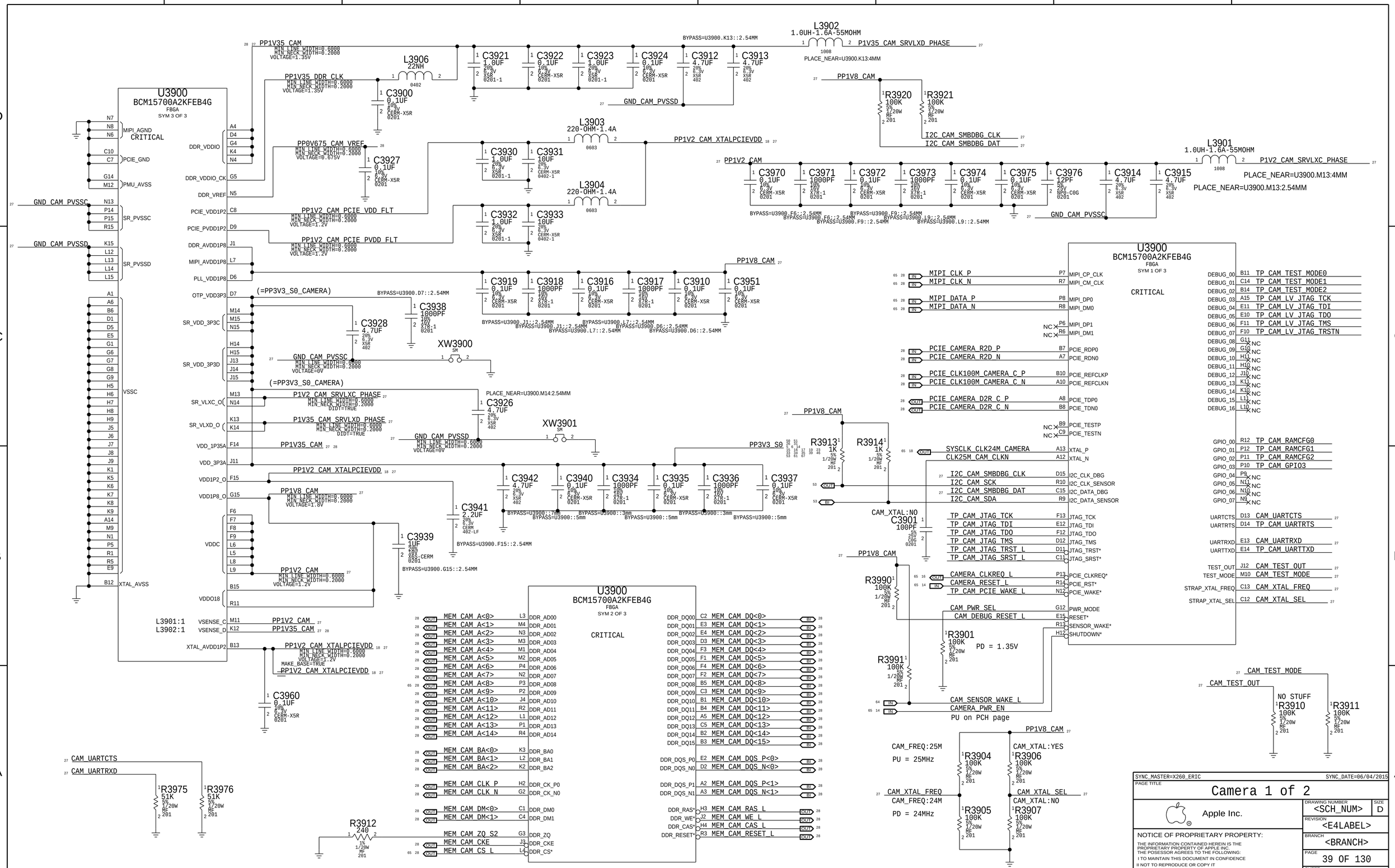
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BCM15700A2KFEB4G
FBGA
SYM 3 OF 3
CRITICAL
U3900
BCM15700A2KFEB4G
FBGA
SYM 1 OF 3
CRITICAL
U3900
BCM15700A2KFEB4G
FBGA
SYM 2 OF 3
CRITICAL
L3902
1.0UH-1.6A-55MOHM
L3901
1.0UH-1.6A-55MOHM
L3906
22NH
L3903
220-OHM-1.4A
L3904
220-OHM-1.4A
PP1V35 CAM
PP1V35 DDR CLK
PP0V675 CAM VREF
PP1V2 CAM PCIE VDD FLT
PP1V2 CAM PCIE PVDD FLT
PP1V2 CAM XTALPCIEVDD
PP1V8 CAM
PP1V2 CAM
P1V35 CAM SRVLXD PHASE
P1V2 CAM SRVLXC PHASE
P1V2 CAM SRVLXC PHASE
PP1V35 CAM
PP3V3 S0
GND CAM PVSSD
(=PP3V3_S0_CAMERA)
XW3900
XW3901
MIPI_AGND
PCIE_GND
PMU_AVSS
SR_PVSSC
SR_PVSSD
VSSC
XTAL_AVSS
DDR_VDDIO
DDR_VDDIO_CK
DDR_VREF
PCIE_VDD1P2
PCIE_PVDD1P2
DDR_AVDD1P8
MIPI_AVDD1P8
PLL_VDD1P8
OTP_VDD3P3
SR_VDD_3P3C
SR_VDD_3P3D
SR_VLXC_O
SR_VLXD_O
VDD_1P35A
VDD_3P3A
VDD1P2_O
VDD1P8_O
VDDC
VDDO18
VSENSE_C
VSENSE_D
XTAL_AVDD1P2
L3901:1
L3902:1
DDR_AD00
DDR_AD01
DDR_AD02
DDR_AD03
DDR_AD04
DDR_AD05
DDR_AD06
DDR_AD07
DDR_AD08
DDR_AD09
DDR_AD10
DDR_AD11
DDR_AD12
DDR_AD13
DDR_AD14
DDR_BA0
DDR_BA1
DDR_BA2
DDR_CK_P0
DDR_CK_N0
DDR_DM0
DDR_DM1
DDR_ZQ
DDR_CKE
DDR_CS*
DDR_DQ00
DDR_DQ01
DDR_DQ02
DDR_DQ03
DDR_DQ04
DDR_DQ05
DDR_DQ06
DDR_DQ07
DDR_DQ08
DDR_DQ09
DDR_DQ10
DDR_DQ11
DDR_DQ12
DDR_DQ13
DDR_DQ14
DDR_DQ15
DDR_DQS_P0
DDR_DQS_N0
DDR_DQS_P1
DDR_DQS_N1
DDR_RAS*
DDR_WE*
DDR_CAS*
DDR_RESET*
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MEM CAM WE L
MEM CAM CAS L
MEM CAM RESET L
MIPI CLK P
MIPI CLK N
MIPI DATA P
MIPI DATA N
PCIE CAMERA R2D P
PCIE CAMERA R2D N
PCIE CLK100M CAMERA C P
PCIE CLK100M CAMERA C N
PCIE CAMERA D2R C P
PCIE CAMERA D2R C N
SYSCLK CLK24M CAMERA
CLK25M CAM CLKN
I2C CAM SMBDBG CLK
I2C CAM SCK
I2C CAM SMBDBG DAT
I2C CAM SDA
TP CAM JTAG TCK
TP CAM JTAG TDI
TP CAM JTAG TDO
TP CAM JTAG TMS
TP CAM JTAG TRST L
TP CAM JTAG SRST L
CAMERA CLKREQ L
CAMERA RESET L
TP CAM PCIE WAKE L
CAM PWR SEL
CAM DEBUG RESET L
CAM SENSOR WAKE L
CAMERA PWR EN
PU on PCH page
PD = 1.35V
CAM_FREQ:25M
PU = 25MHz
CAM_FREQ:24M
PD = 24MHz
CAM_XTAL:YES
CAM_XTAL:NO
CAM_XTAL:NO
CAM_XTAL FREQ
CAM_XTAL SEL
CAM UARTCTS
CAM UARTRXD
CAM TEST MODE
CAM TEST OUT
NO STUFF
TP CAM TEST MODE0
TP CAM TEST MODE1
TP CAM TEST MODE2
TP CAM LV JTAG TCK
TP CAM LV JTAG TDI
TP CAM LV JTAG TDO
TP CAM LV JTAG TMS
TP CAM LV JTAG TRSTN
TP CAM RAMCFG0
TP CAM RAMCFG1
TP CAM RAMCFG2
TP CAM GPIO3
CAM UARTCTS
TP CAM UARTRTS
CAM UARTRXD
TP CAM UARTTXD
CAM TEST OUT
CAM TEST MODE
CAM XTAL FREQ
CAM XTAL SEL
SYNC_MASTER=X260_ERIC
SYNC_DATE=06/04/2015
PAGE TITLE
Camera 1 of 2
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
BRANCH
<BRANCH>
PAGE
39 OF 130
SHEET
27 OF 67
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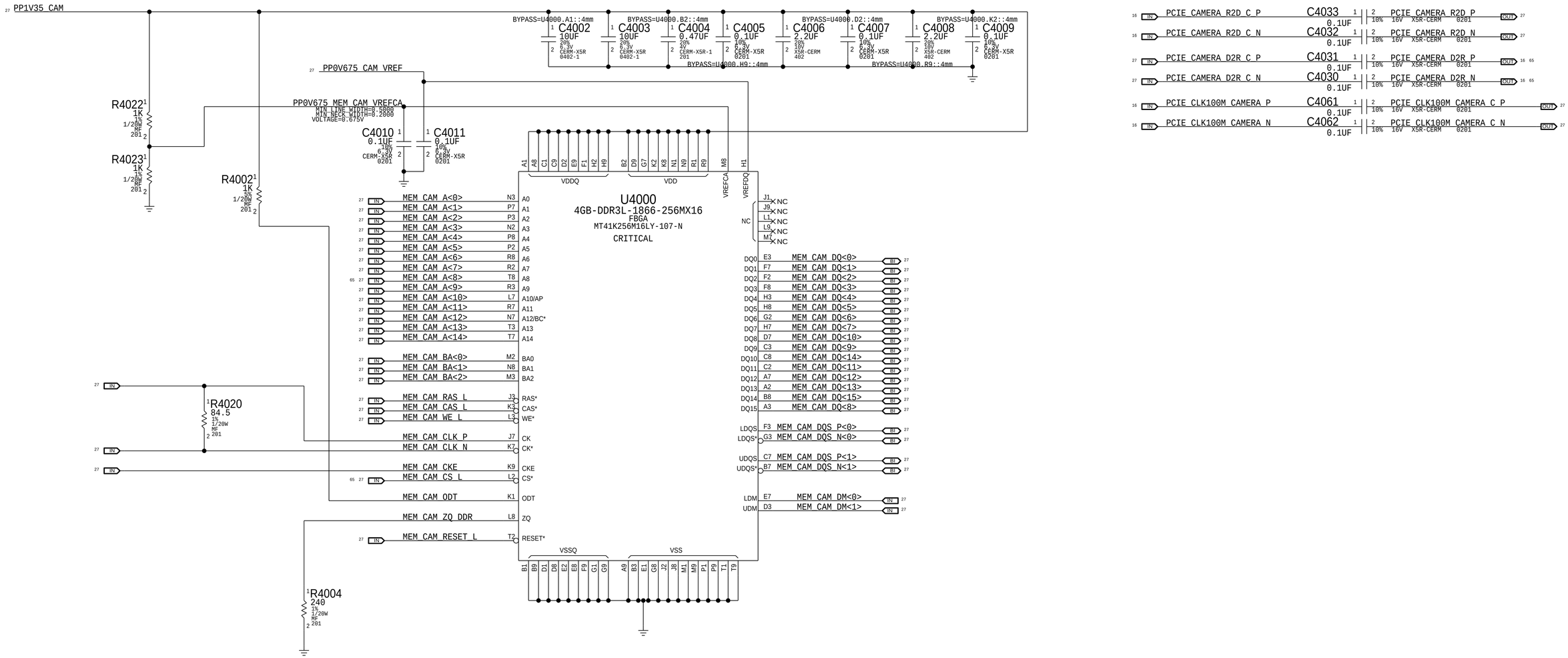
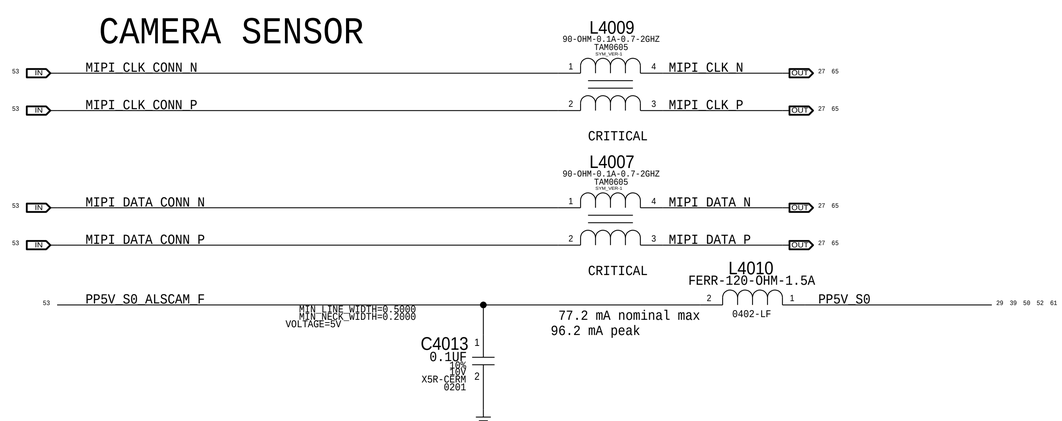


CAMERA SENSOR



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PAGE TITLE: Camera 2 of 2	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
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	SHEET: 28 OF 67

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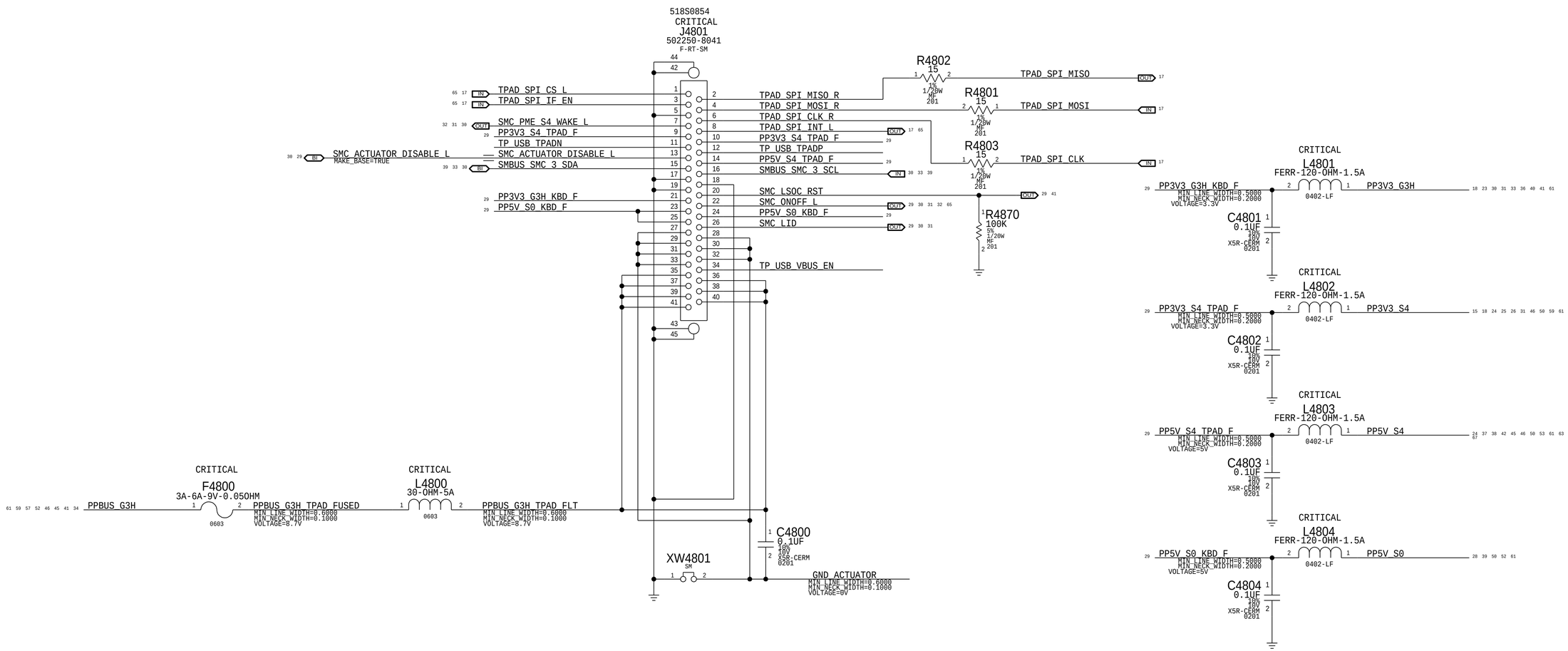
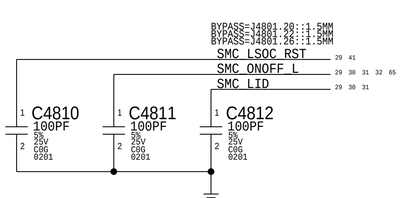
IPD ZIF CONNECTOR

Bottom side contacts used
Pinout reversed from flex





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PAGE TITLE
Keyboard & Trackpad Conn

Apple Inc.

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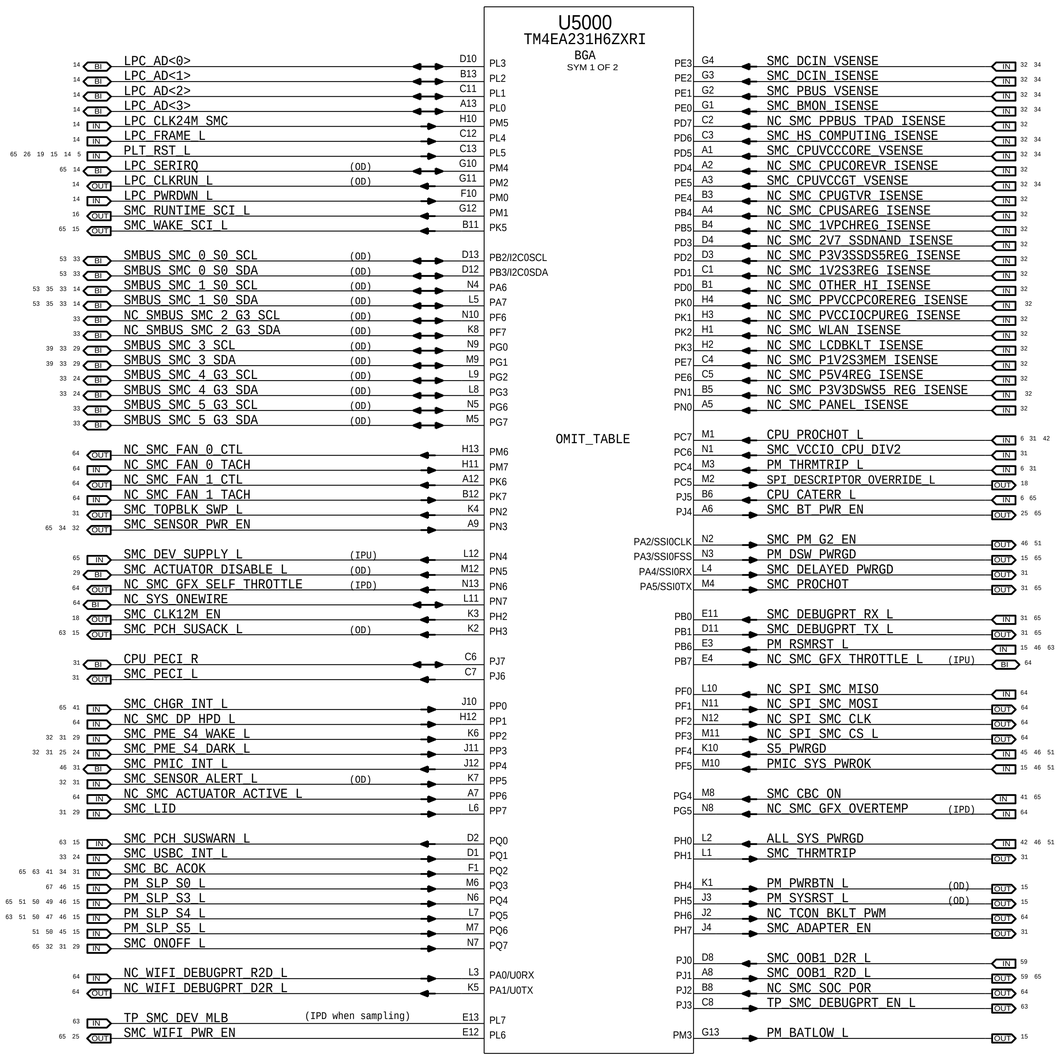
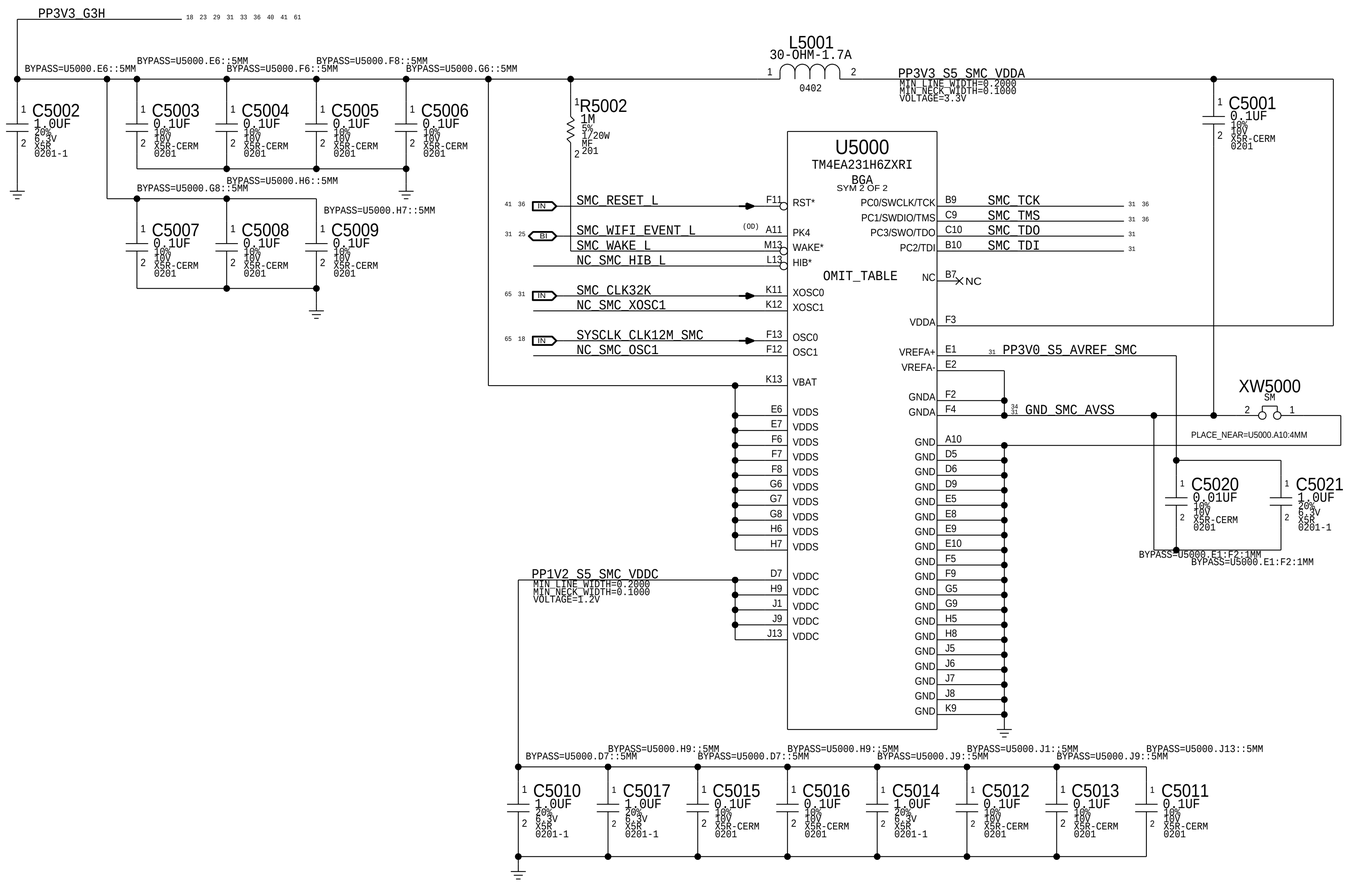


NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.



PAGE TITLE	SMC
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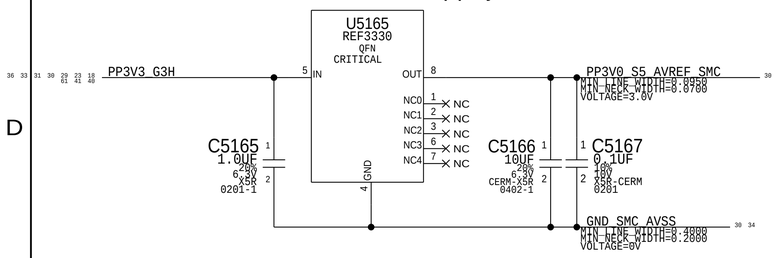
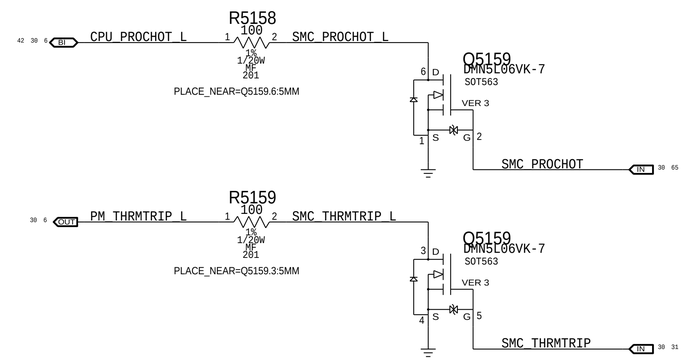
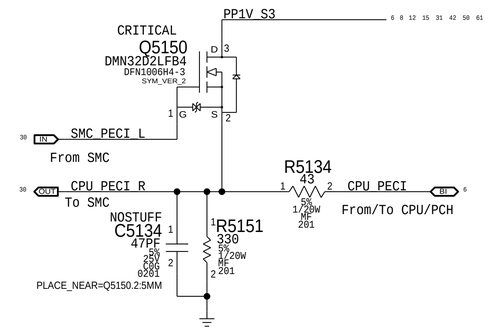
SMC AVREF Supply



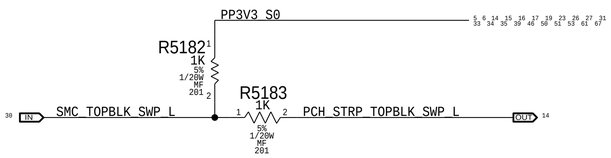
PROCHOT/THRMTRIP Support

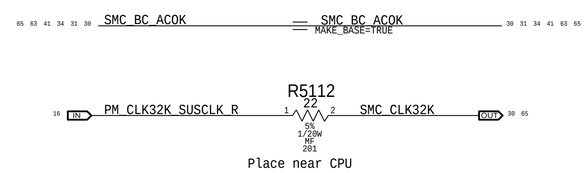


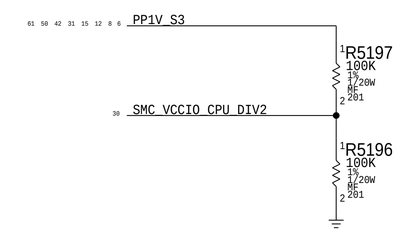
PECI Support

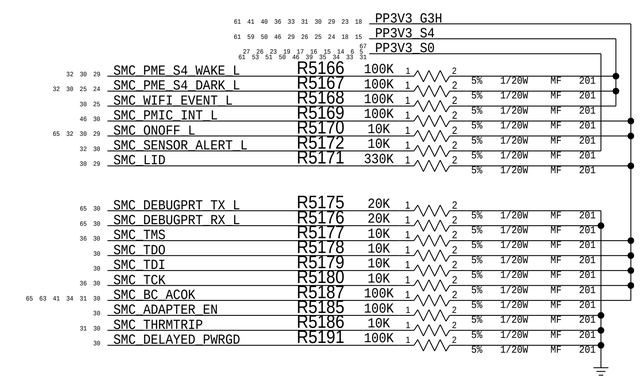


Top-Block Swap









SYNC_MASTER=X260_ERIC SYNC_DATE=06/04/2015

PAGE TITLE

SMC Shared Support

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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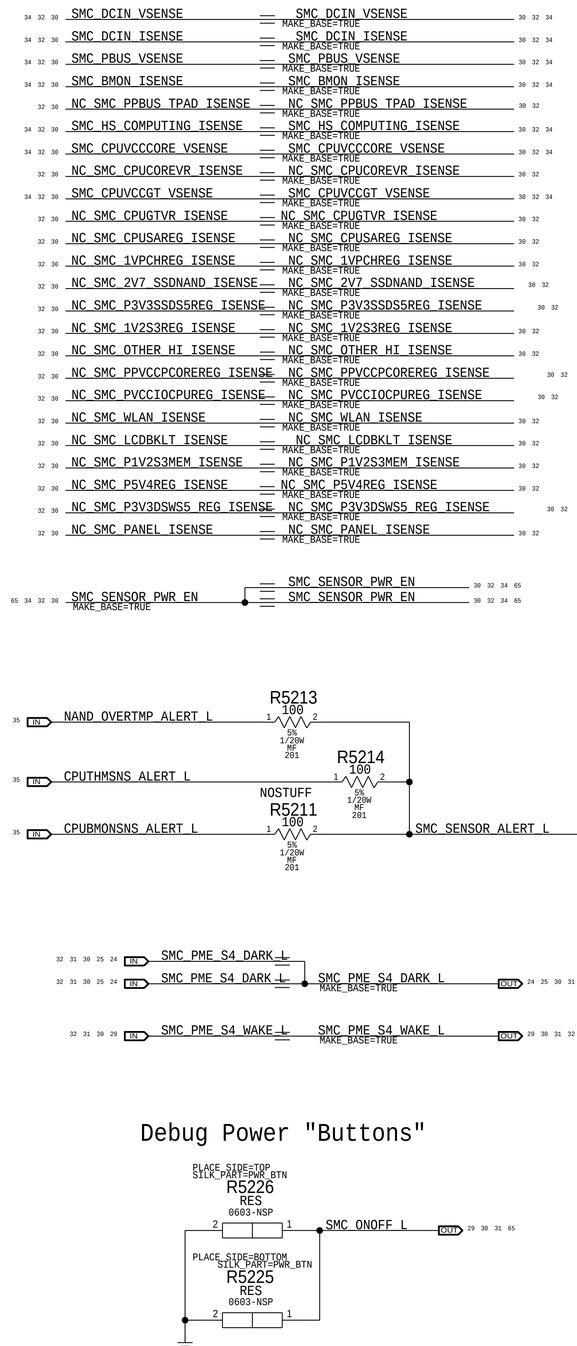

Debug Power "Buttons"

SYNC_MASTER=X260_ERIC SYNC_DATE=06/04/2015

PAGE TITLE

SMC Project Support

Apple Inc.

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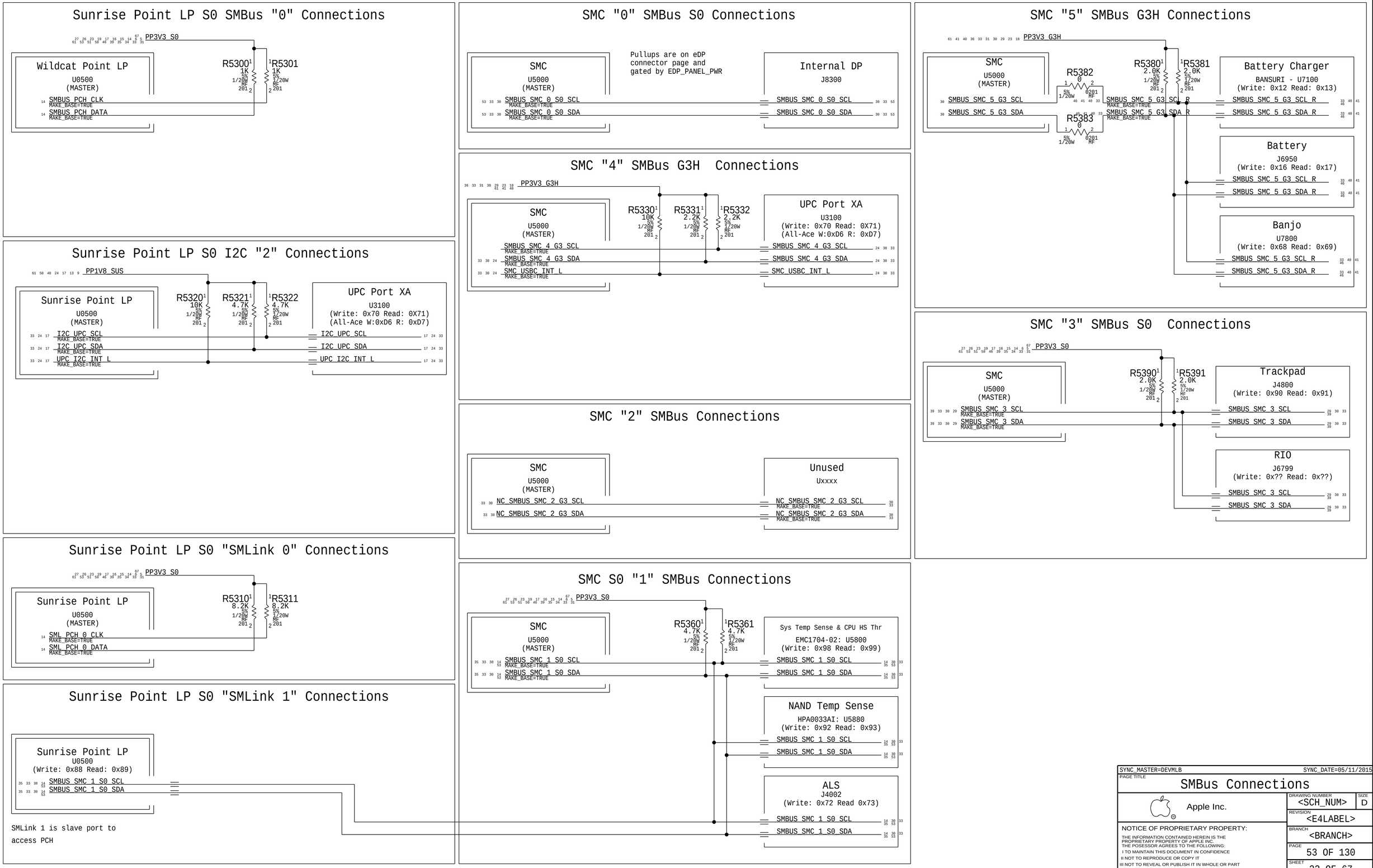

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PAGE TITLE

SMBus Connections

Apple Inc.

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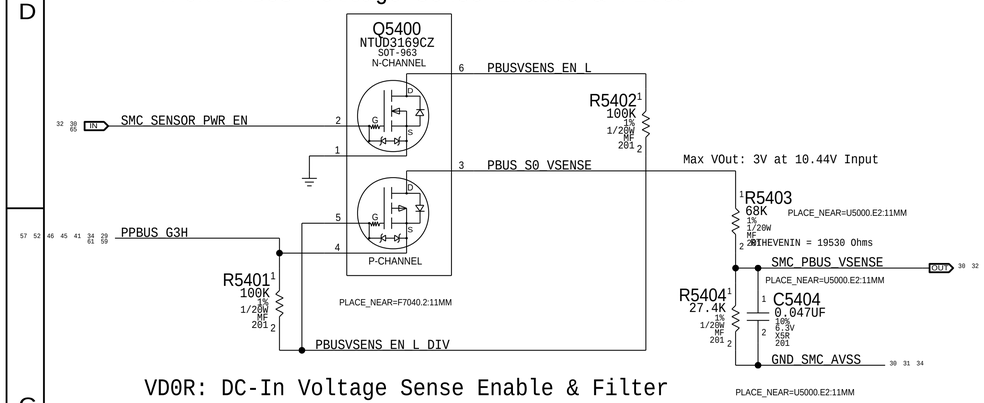
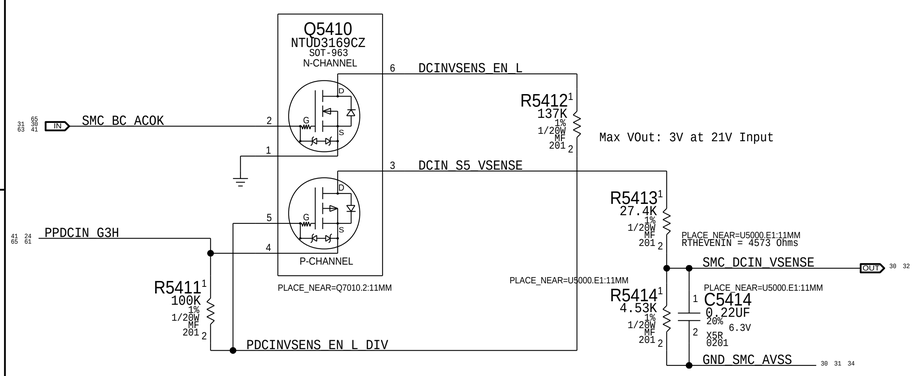
POR VOLTAGE / CURRENT SENSORS : TO BE USED IN PRODUCTION

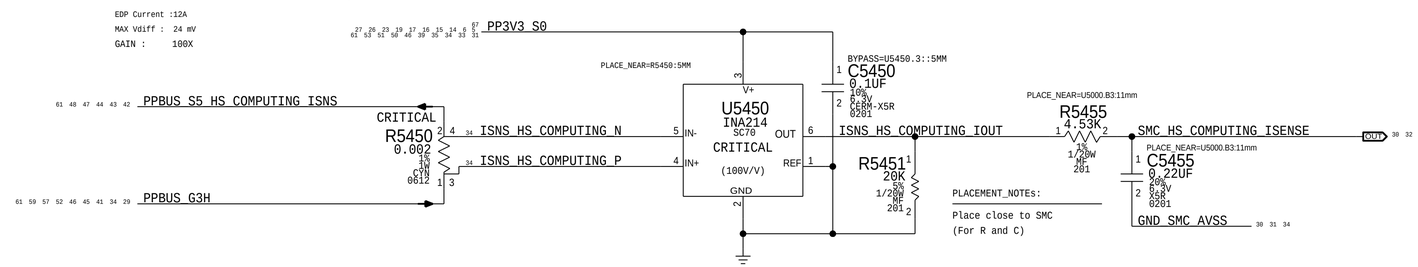
VP0R: PBUS Voltage Sense Enable & Filter



VD0R: DC-In Voltage Sense Enable & Filter

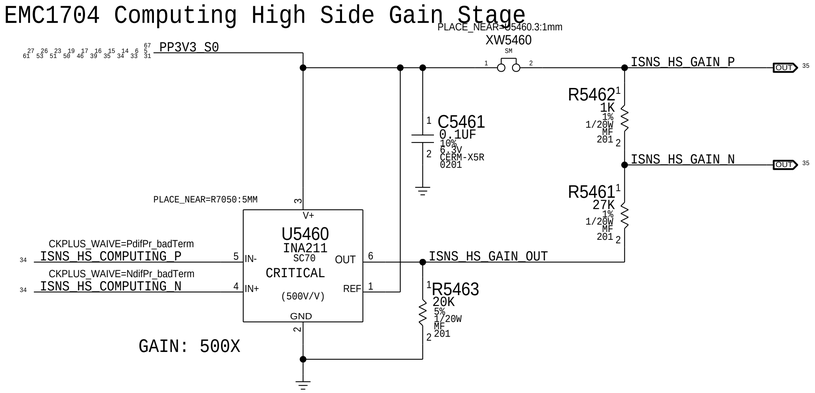


IC0R : COMPUTING High Side Current Sense

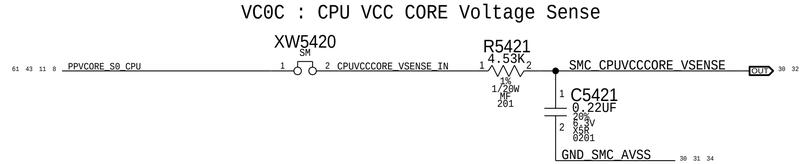


Need to set gains for ULX

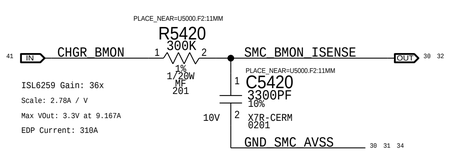
EMC1704 Computing High Side Gain Stage



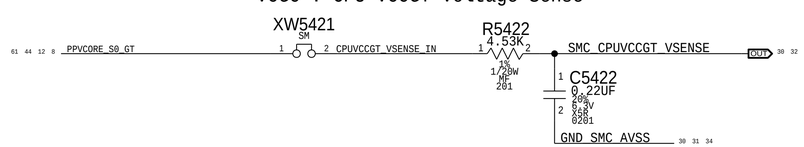
VC0C : CPU VCC CORE Voltage Sense



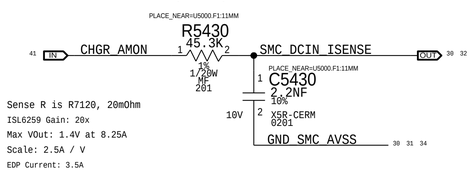
CHARGER BMON High Side Current Sense



VCGC : CPU VCCGT Voltage Sense



DC-IN (AMON) Current Sense



SYNC_MASTER=DEVMLB SYNC_DATE=07/06/2015

PAGE TITLE: Voltage & Current Sensing

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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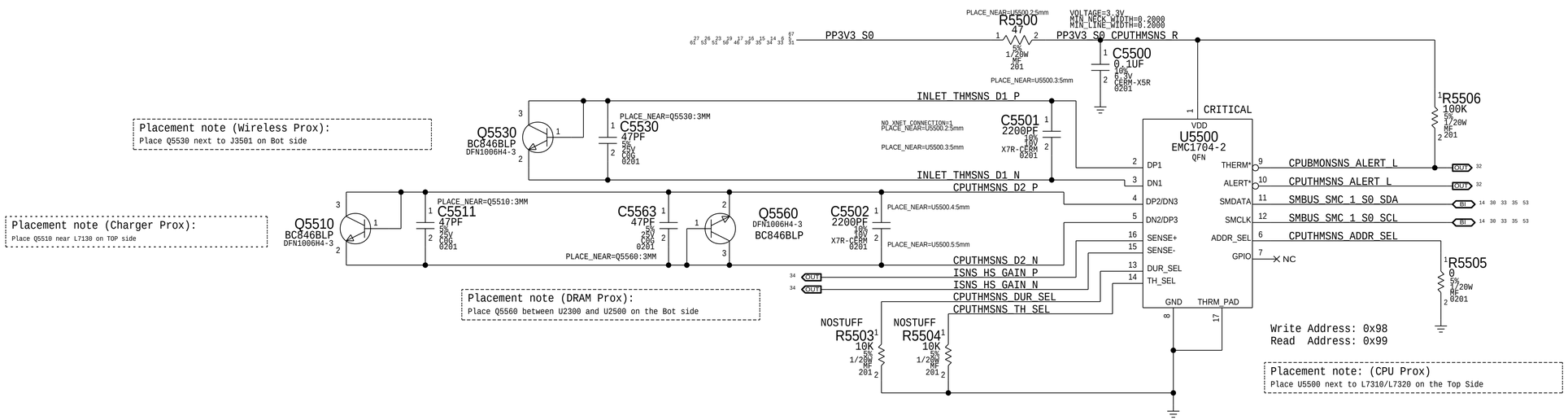
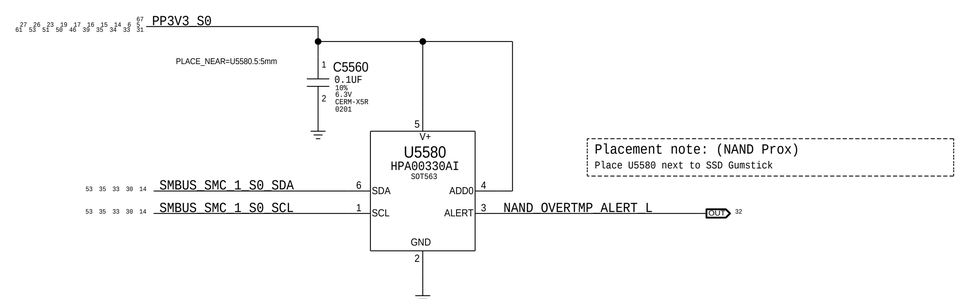
POR THERMAL SENSORS : TO BE USED IN PRODUCTION

CPU Proximity, Inlet ,DDR and BMON THR Sensor



NAND Temp Sensor



SENSORS

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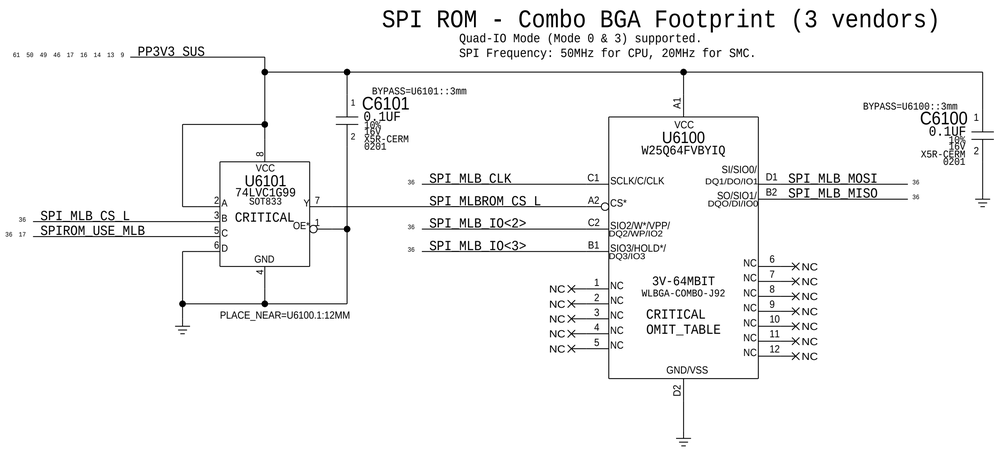

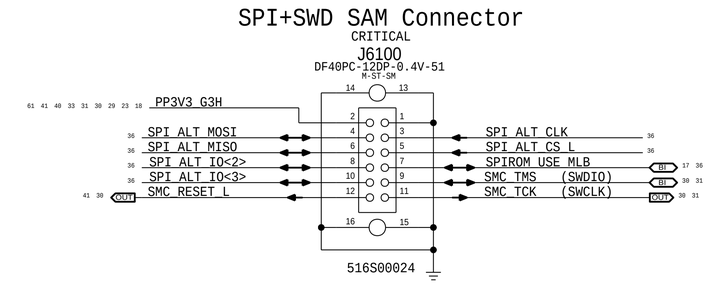

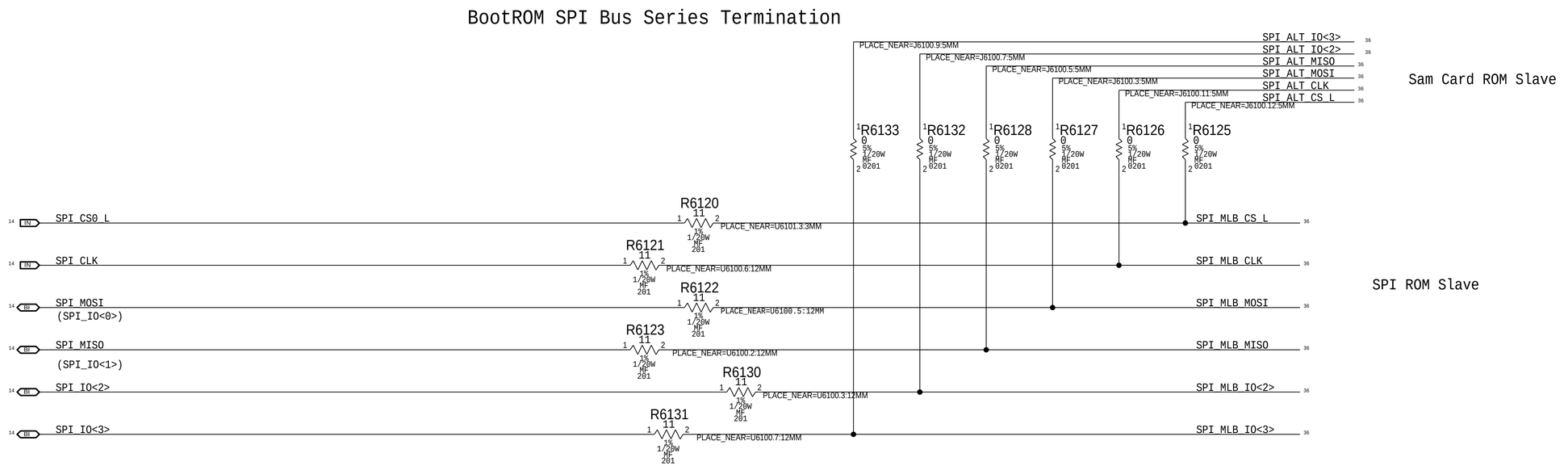

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PAGE TITLE
SPI+SWD Debug Connector

Apple Inc.

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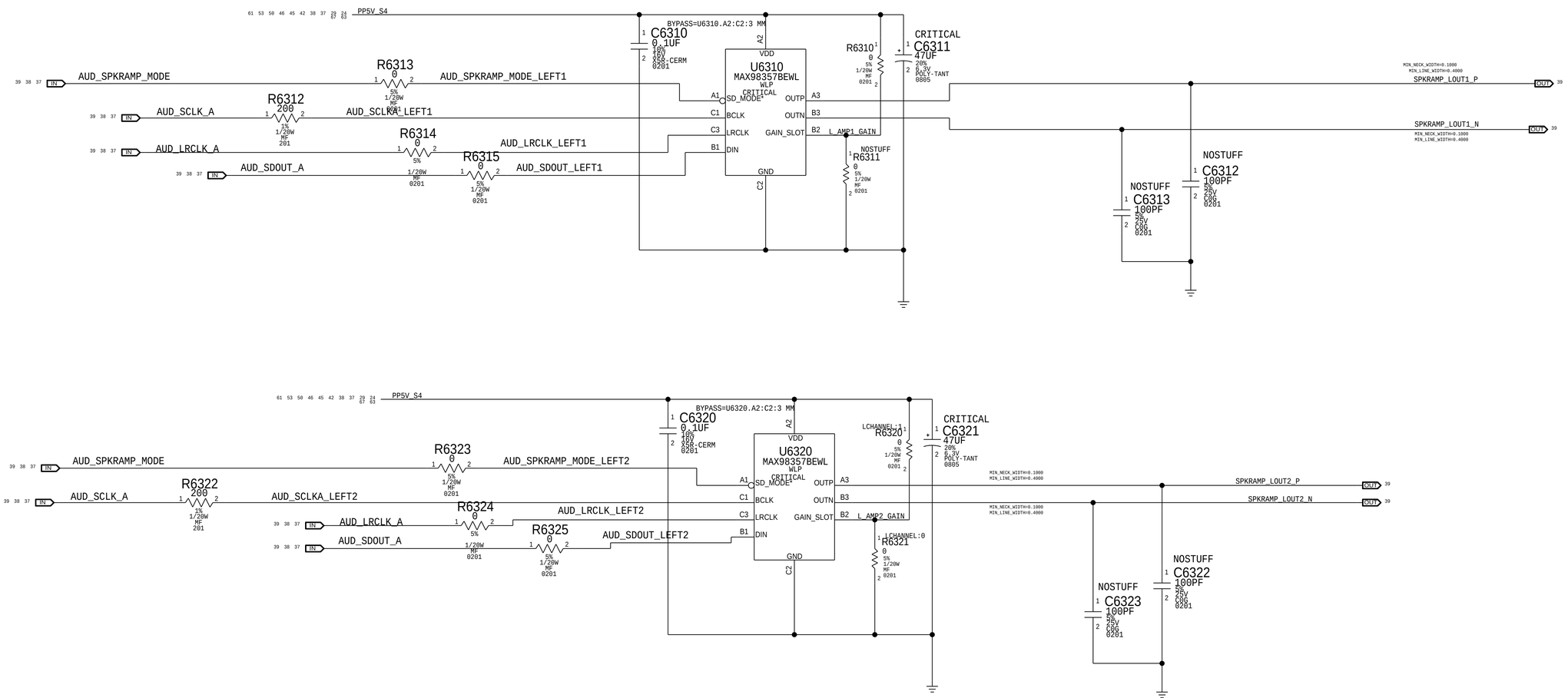
Left Speaker Amps

APPLE P/N 353S4265



SPEAKER CONFIGS

BOM GROUP	BOM OPTIONS
EQ:2CH	LCHANNEL:1,RCHANNEL:3
EQ:4CH	LCHANNEL:0,RCHANNEL:4

SYNC_MASTER=J92_DEVMLB SYNC_DATE=09/19/2013

PAGE TITLE
AUDIO Left Speaker Amps

Apple Inc.

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REVISION <E4LABEL>

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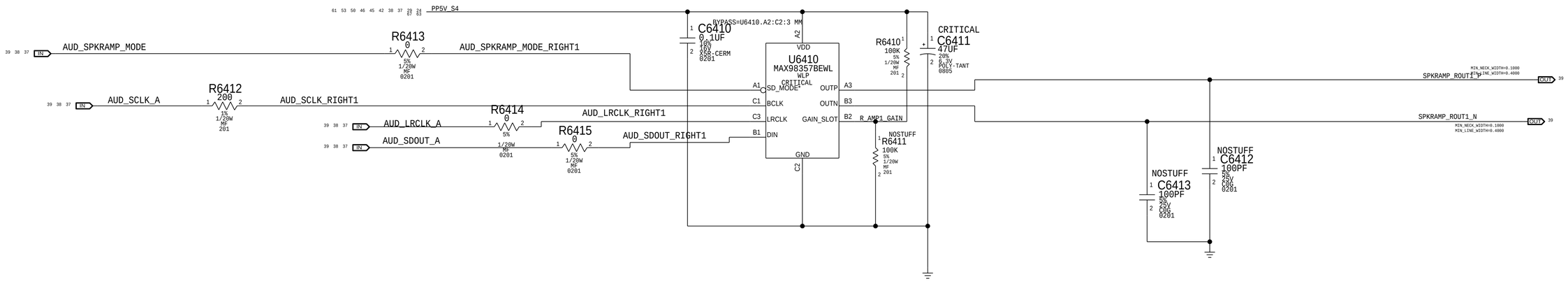
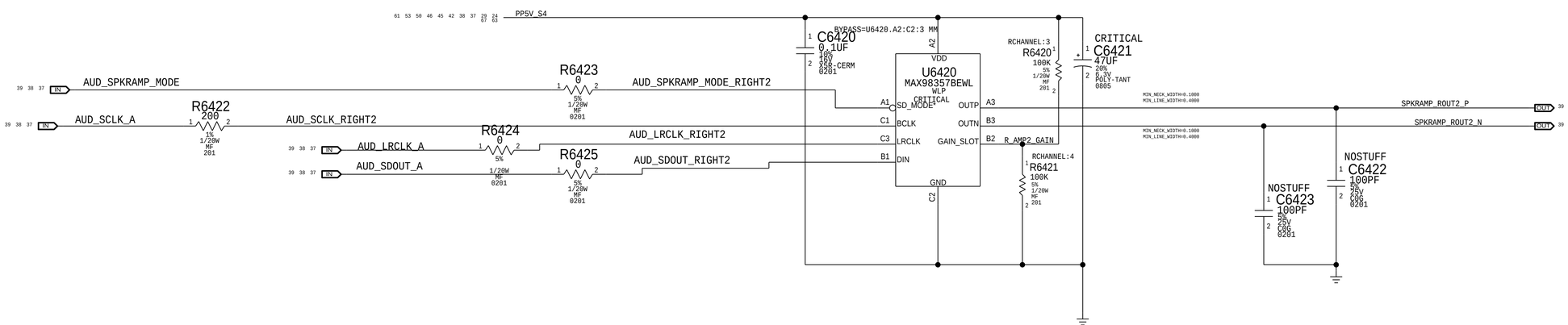
Right Speaker Amps

APPLE P/N 353S4265





SYNC_MASTER=J92_DEVMLB SYNC_DATE=09/19/2013

PAGE TITLE
AUDIO Right Speaker Amps

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)		0X09 (A)
SPEAKERS	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A

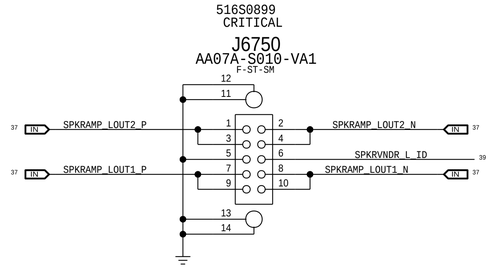
CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

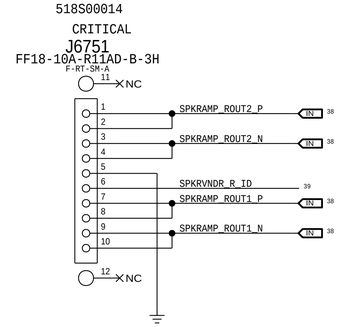
SOUTHBRIDGE RESOURCE/PIN ALLOCATIONS

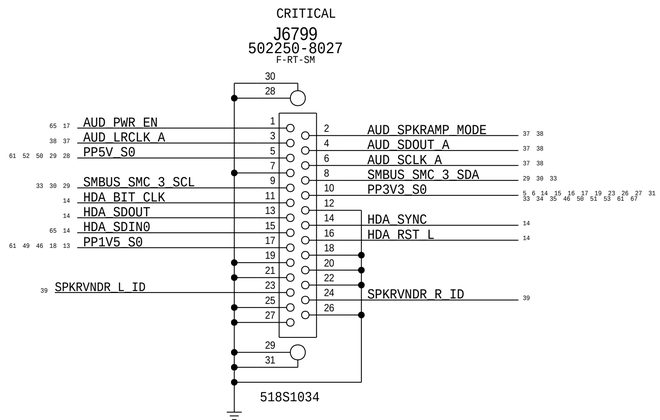
FUNCTION	NET NAME	SB GPIO/INT
PERIPHERAL/EXTRACTION DETECT	AUD_IP_PERIPHERAL_DET	GPIO 3
MIKEY INTERRUPT	AUD_I2C_INT_L	GPIO 5
MIKEY ENABLE	AUD_IPHS_SWITCH_EN	GPIO 16
MIKEY I2C BUS	I2C_MIKEY_SDA/SCL	PCH SMBUS 0

LEFT SPEAKER CONN



RIGHT SPEAKER CONN





RIO FLEX CONN

SYNC_MASTER=CARA_J92 SYNC_DATE=04/17/2014

PAGE TITLE
AUDIO CONNECTORS

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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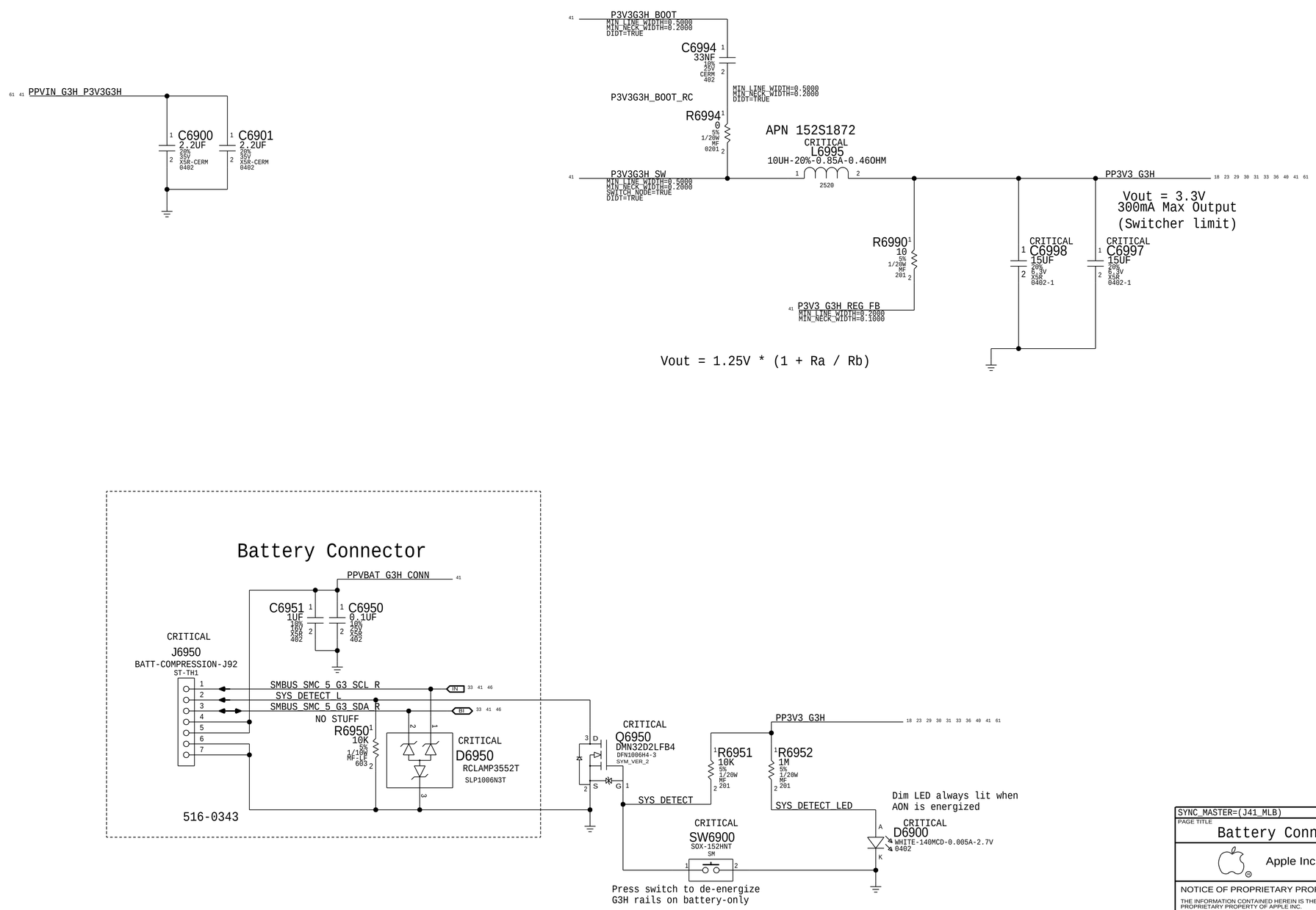
3.3V G3H VR - Bansuri



SYNC_MASTER=(J41_MLB)	SYNC_DATE=03/16/2015
PAGE TITLE: Battery Connector & 3.3V G3Hot	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
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	SHEET: 40 OF 67

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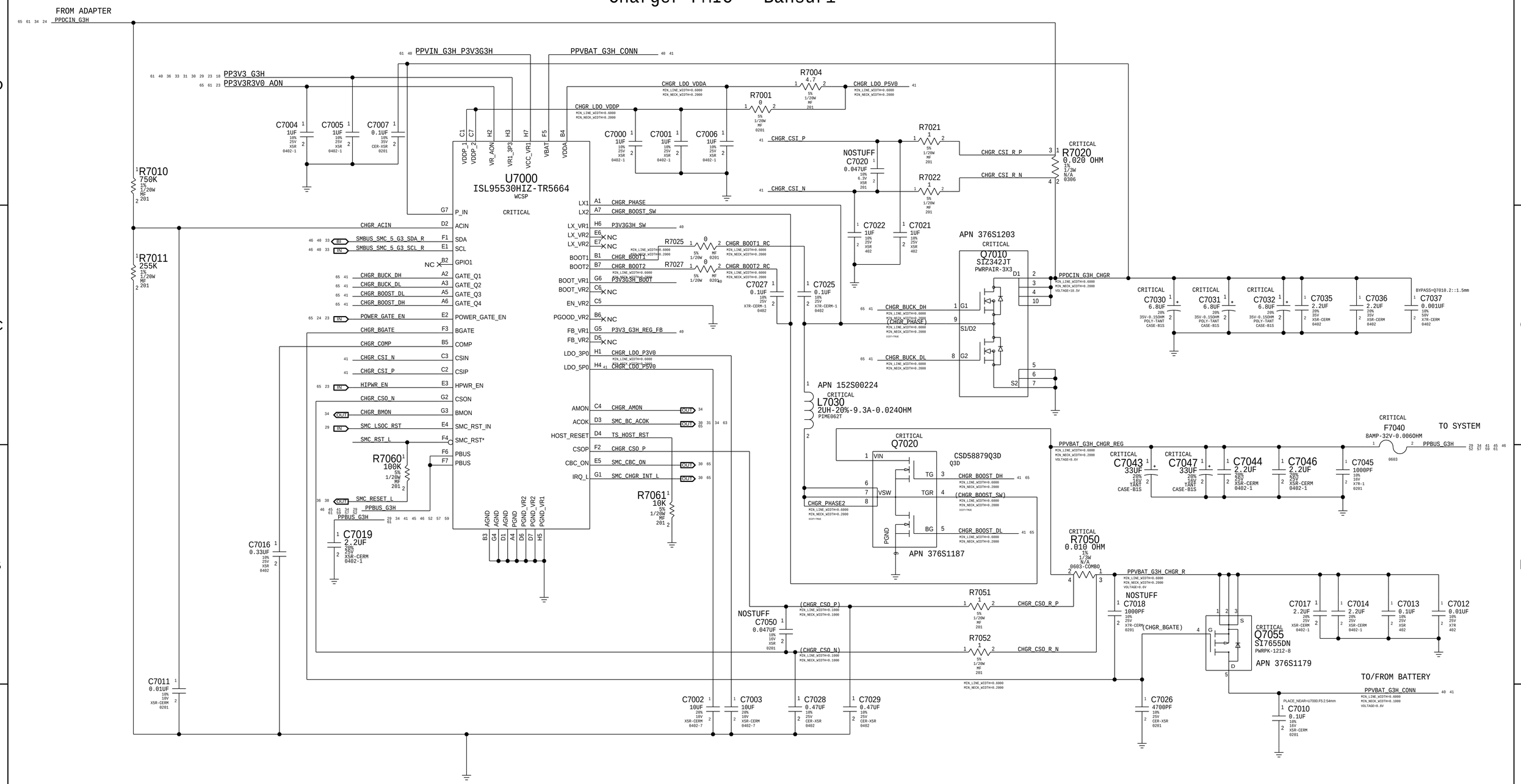
Charger PMIC - Bansuri



SYNC_MASTER=DEVMLB SYNC_DATE=05/11/2015

PAGE TITLE

PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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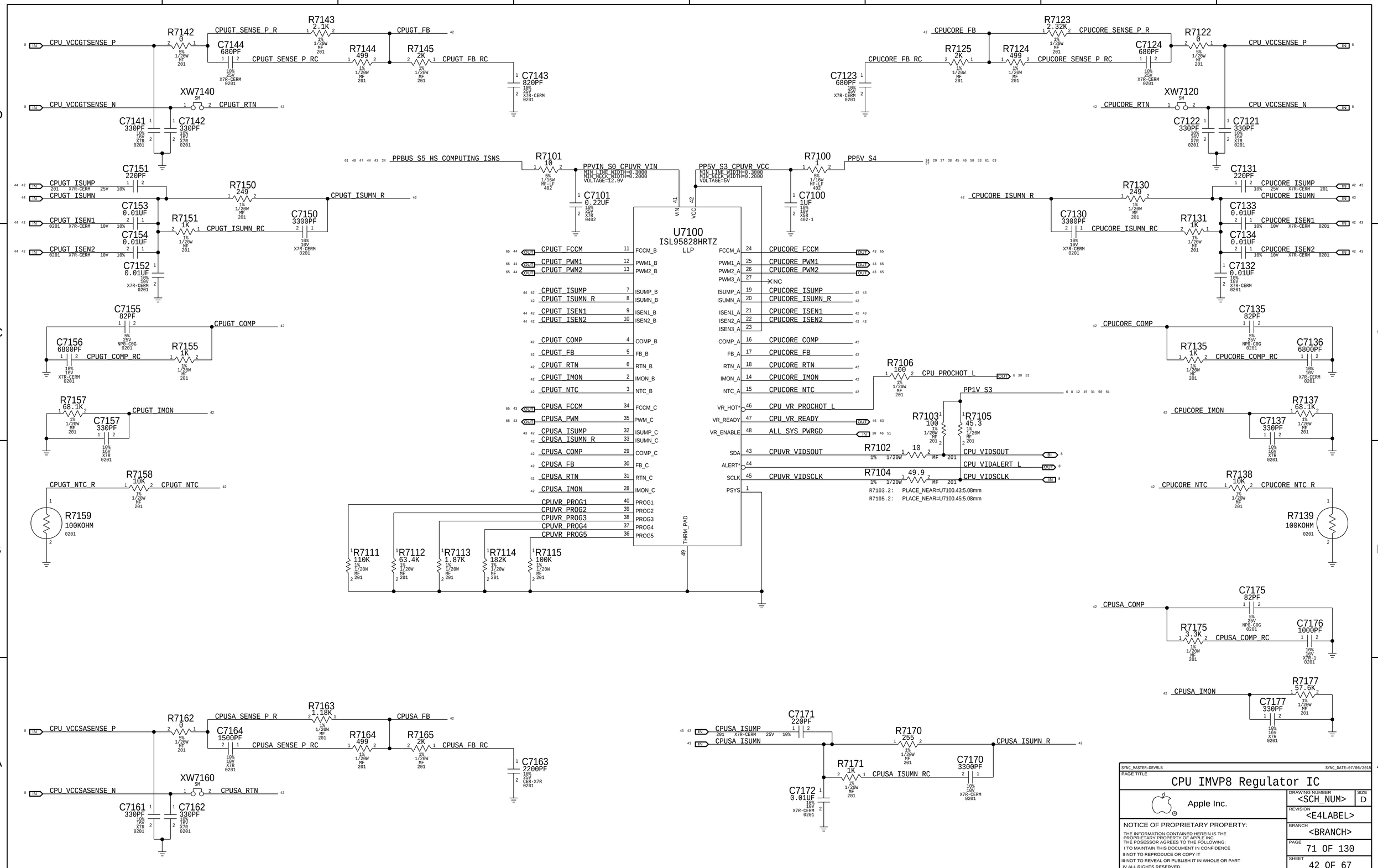

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Note:Vcore design requires 4x POSCAPs
3x shared from other VRs

Phase 1

PPBUS S5 HS COMPUTING ISNS

CRITICAL C7210 33UF 20% 16V TANT CASE-B1S
CRITICAL C7211 33UF 20% 16V TANT CASE-B1S
C7214 2.2UF 20% 25V X6S-CERM 0402
C7215 2.2UF 20% 25V X6S-CERM 0402

PP5V_S0_CPUCORE1 MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.2000 VOLTAGE=5V

R7217 2.2 1% 1/20W MF 201

PP5V_S4RS0

C7217 2.2UF 20% 25V X6S-CERM 0402

C7216 2.2UF 20% 25V X6S-CERM 0402

U7210 SIC535CD MLP4535

VIN, VCIN, VDRV, ZCD_EN*, PWM, NC, BOOT, PHASE, VSWH, GL, PGND, CGND

CPUCORE_FCCM
CPUCORE_PWM1

CRITICAL

XW7210 SM

GND_CPUCORE1_CGND MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.2000 VOLTAGE=0V

CPUCORE_BOOT1_R MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.2000 DIDT=TRUE

R7219 0 5% 1/16W MF-LF 402

C7219 0.22UF 10% 25V X7R 0402

CPUCORE_BOOT1 MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.2000 DIDT=TRUE
CPUCORE_BOOT1_RC MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.2000 DIDT=TRUE
CPUCORE_PHASE1 MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.2000 DIDT=TRUE SWITCH_NODE=TRUE
CPUCORE_GL1

CRITICAL L7210 0.22UH-20%-12A-0.0045OHM PILE052T-SM 152S00217

PPVCORE_S0_CPU_PH1 MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.2000 VOLTAGE=1.5V

CRITICAL R7210 0.001 1% 1/2W MF 0306

CPUCORE_ISNS1_P
CPUCORE_ISNS1_N

NO_XNET_CONNECTION=1 R7214 2.2 1% 1/20W MF 201 CPUCORE_ISUMN

NO_XNET_CONNECTION=1 R7211 1K 1% 1/20W MF 201

NO_XNET_CONNECTION=1 R7212 200K 1% 1/20W MF 201

R7213 200K 1% 1/20W MF 201 CPUCORE_ISNS2_N

NO_XNET_CONNECTION=1

CPUCORE_ISEN1
CPUCORE_ISUMP

PPVCORE_S0_CPU

Vout = 1.50V max
24A max load
f = 750kHz

Phase 2

PPBUS S5 HS COMPUTING ISNS

CRITICAL C7230 33UF 20% 16V TANT CASE-B1S
CRITICAL C7231 33UF 20% 16V TANT CASE-B1S
C7234 2.2UF 20% 25V X6S-CERM 0402
C7235 2.2UF 20% 25V X6S-CERM 0402

PP5V_S0_CPUCORE2 MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.2000 VOLTAGE=5V

R7237 2.2 1% 1/20W MF 201

PP5V_S4RS0

C7237 2.2UF 20% 25V X6S-CERM 0402

C7236 2.2UF 20% 25V X6S-CERM 0402

U7230 SIC535CD MLP4535

VIN, VCIN, VDRV, ZCD_EN*, PWM, NC, BOOT, PHASE, VSWH, GL, PGND, CGND

CPUCORE_FCCM
CPUCORE_PWM2

CRITICAL

XW7230 SM

GND_CPUCORE2_CGND MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.2000 VOLTAGE=0V

CPUCORE_BOOT2_R MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.2000 DIDT=TRUE

R7239 0 5% 1/10W MF-LF 402

C7239 0.22UF 10% 25V X7R 0402

CPUCORE_BOOT2 MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.2000 DIDT=TRUE
CPUCORE_BOOT2_RC MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.2000 DIDT=TRUE
CPUCORE_PHASE2 MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.2000 DIDT=TRUE SWITCH_NODE=TRUE
CPUCORE_GL2

CRITICAL L7230 0.22UH-20%-12A-0.0045OHM PILE052T-SM 152S00217

PPVCORE_S0_CPU_PH2 MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.2000 VOLTAGE=1.5V

CRITICAL R7230 0.001 1% 1/2W MF 0306

CPUCORE_ISNS2_P
CPUCORE_ISNS2_N

NO_XNET_CONNECTION=1 R7234 2.2 1% 1/20W MF 201 CPUCORE_ISUMN

NO_XNET_CONNECTION=1 R7231 1K 1% 1/20W MF 201

NO_XNET_CONNECTION=1 R7232 200K 1% 1/20W MF 201

R7233 200K 1% 1/20W MF 201 CPUCORE_ISNS1_N

NO_XNET_CONNECTION=1

CPUCORE_ISEN2
CPUCORE_ISUMP

CPU VCCSA

PPBUS S5 HS COMPUTING ISNS

CRITICAL C7290 33UF 20% 16V TANT CASE-B1S
C7294 2.2UF 20% 25V X6S-CERM 0402
C7295 2.2UF 20% 25V X6S-CERM 0402

PP5V_S4RS0

C7296 2.2UF 20% 25V X6S-CERM 0402

U7290 ISL6208D DFN

VCC, PWM, FCCM, BOOT, UGATE, PHASE, LGATE, GND, THRM PAD

CPUSA_PWM
CPUSA_FCCM

CRITICAL

CPUSA_BOOT MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.2000 DIDT=TRUE
CPUSA_UGATE MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 DIDT=TRUE GATE_NODE=TRUE
CPUSA_PHASE MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.2000 DIDT=TRUE SWITCH_NODE=TRUE
CPUSA_LGATE MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 DIDT=TRUE GATE_NODE=TRUE

CPUSA_BOOT_R MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.2000 DIDT=TRUE

R7299 0 5% 1/10W MF-LF 402

C7299 0.22UF 10% 25V X7R 0402

CRITICAL Q7291 CSD58873Q3D Q3D

VIN, TG, TGR, VSW, BG, PGND

CPUSA_SW_LL MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 DIDT=TRUE SWITCH_NODE=TRUE

CRITICAL L7290 0.47UH-20%-8.5A-0.0350HM PIMA032T-SM

PPVCCSA_S0_CPU MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.2000 VOLTAGE=1.5V

CRITICAL R7290 0.003 1% 1/2W MF 0306

CPUSA_ISNS_P
CPUSA_ISNS_N

NO_XNET_CONNECTION=1 R7291 1K 1% 1/20W MF 201

NO_XNET_CONNECTION=1 R7292 0 5% 1/20W MF 0201

CPUSA_ISUMN
CPUSA_ISUMP

XW7290 SM PLACE_NEAR=R7290:5MM

PPVCCSA_DDR_S0

PPVCCSA_S0

Vout = 1.05V max
4.1A max load
f = 750kHz

SYNC_MASTER=DEVMLB	SYNC_DATE=05/19/2015
PAGE TITLE	CPU VCore/VccSA Power Stage
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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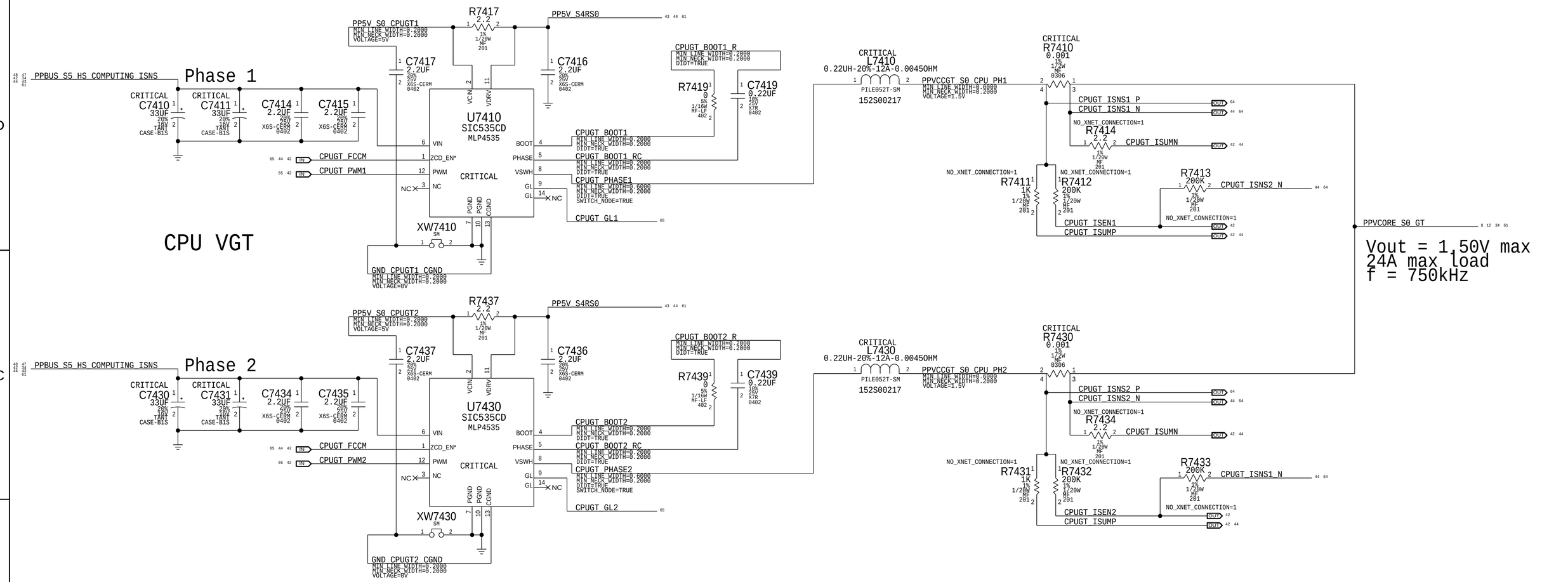

SYNC_MASTER=DEVMLB SYNC_DATE=05/11/2015

PAGE TITLE
CPU VccGT Power Stage

Apple Inc.

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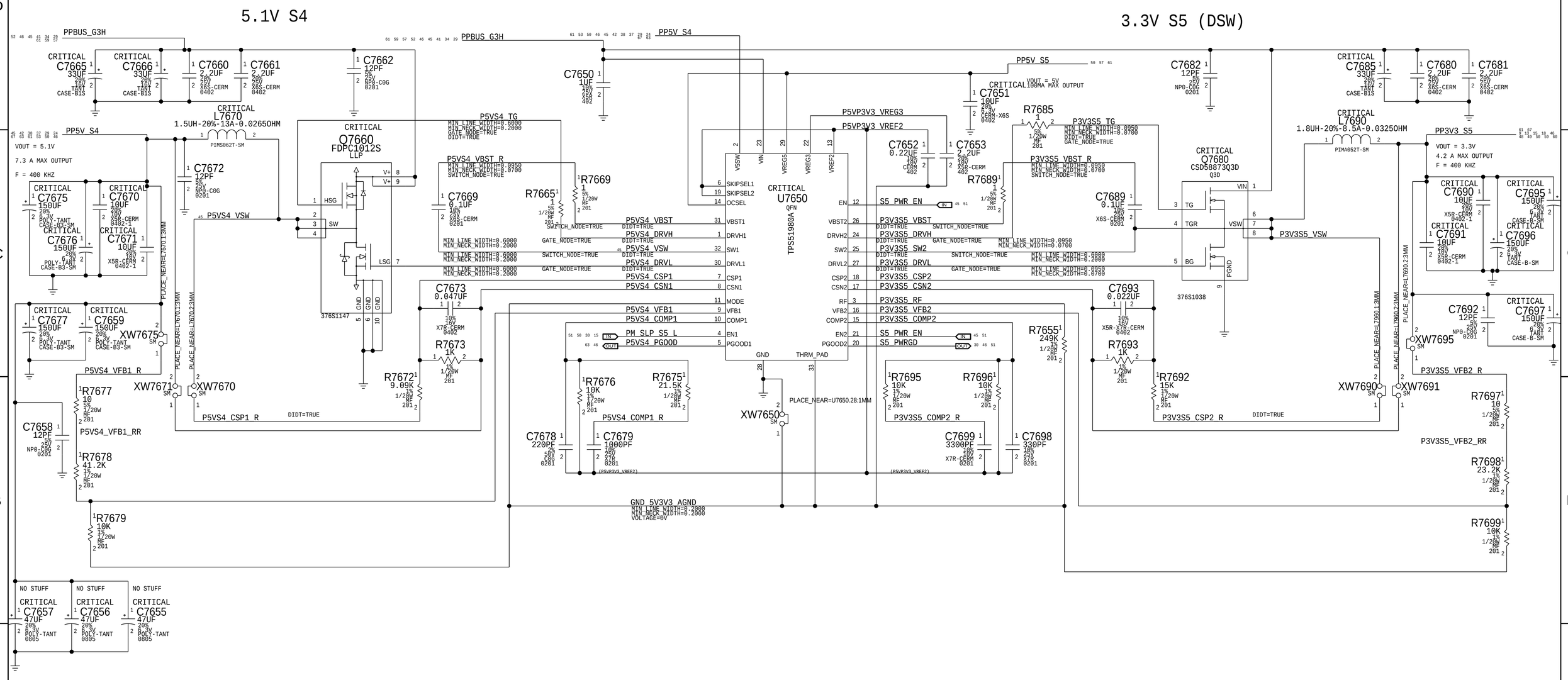

SYNC_MASTER=J92_MLB SYNC_DATE=03/20/2015

PAGE TITLE
5V & 3.3V Power Supplies

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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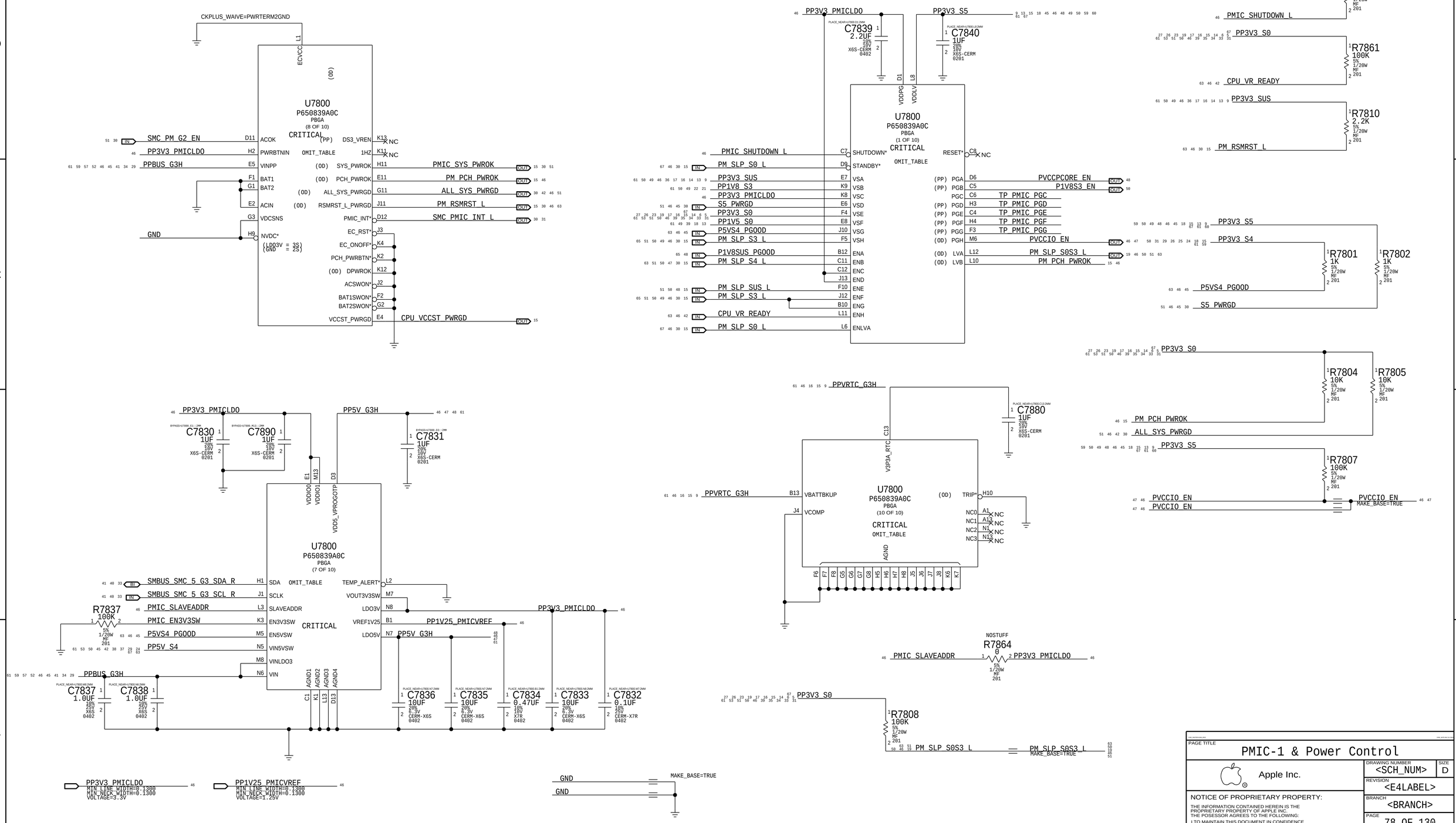
BANJO - PMIC Control



PAGE TITLE

PMIC-1 & Power Control

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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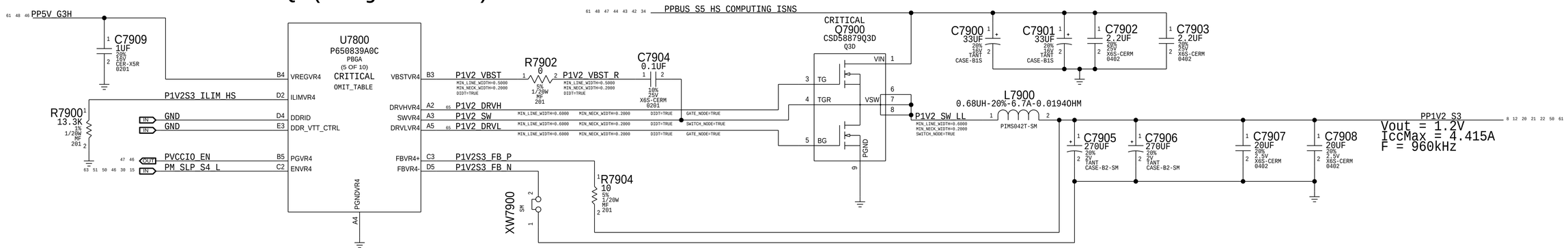
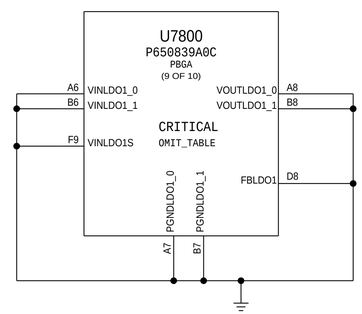
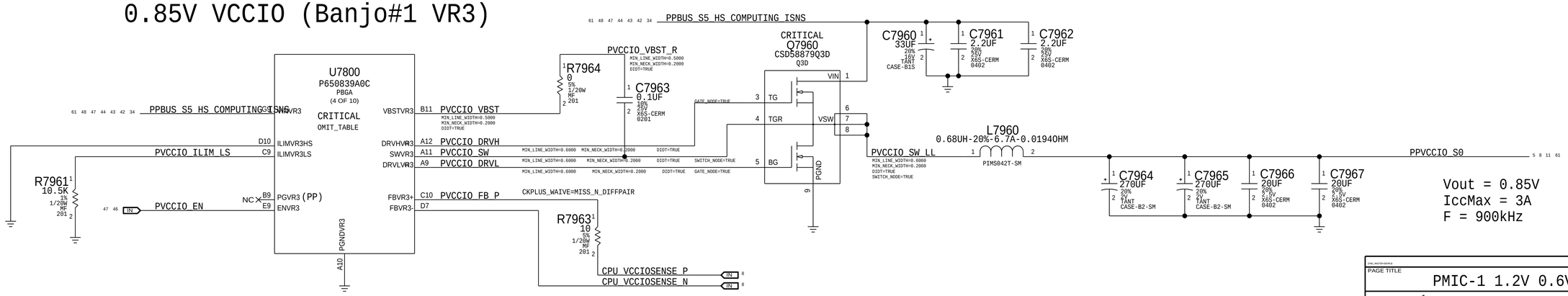
1.2V VDDQ (Banjo#1 VR4)



0.6V VTT (Banjo#1 LDO1)



0.85V VCCIO (Banjo#1 VR3)



PAGE TITLE
PMIC-1 1.2V 0.6V VCCIO

Apple Inc.

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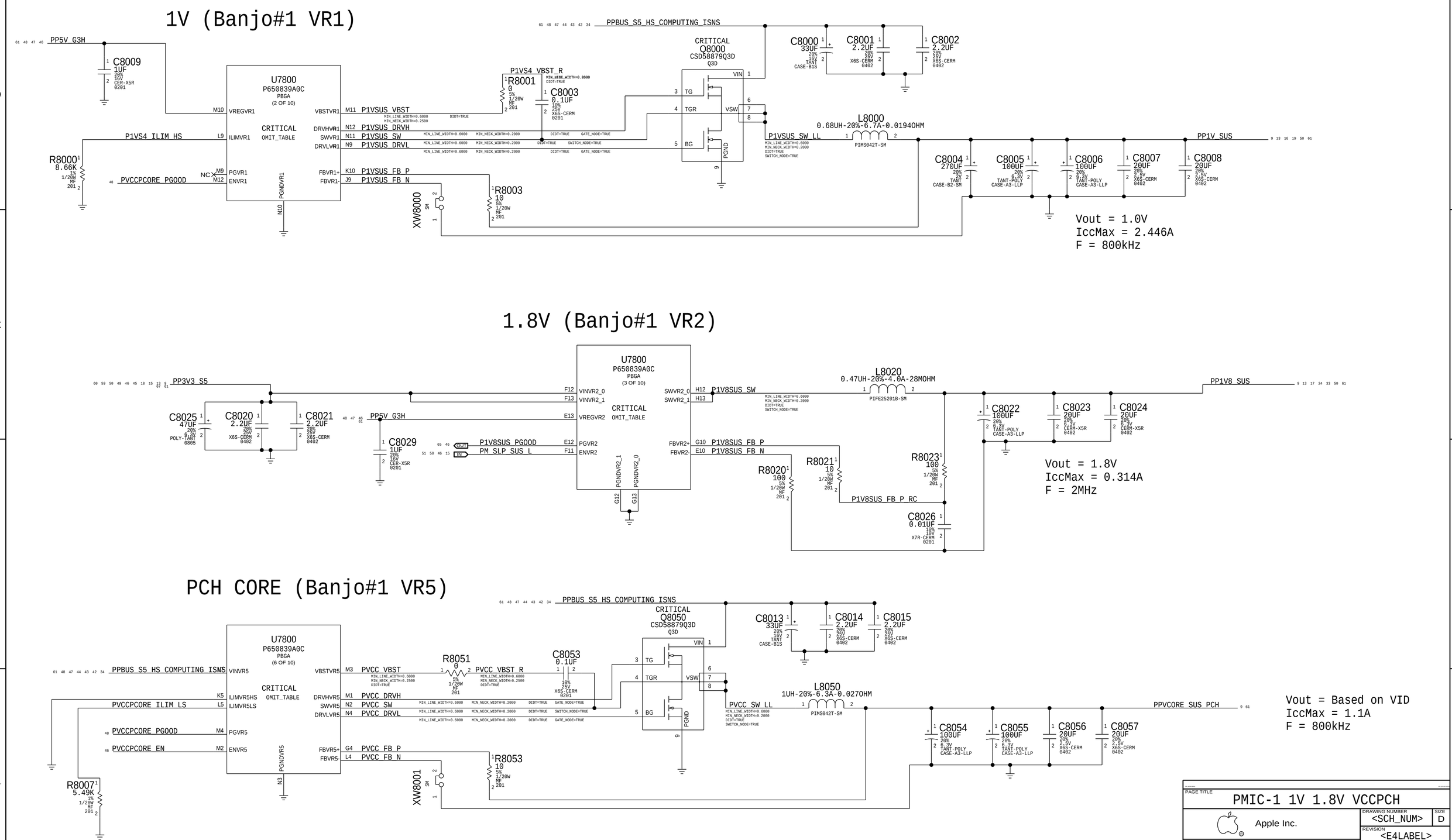

PAGE TITLE
PMIC-1 1V 1.8V VCCPCH

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
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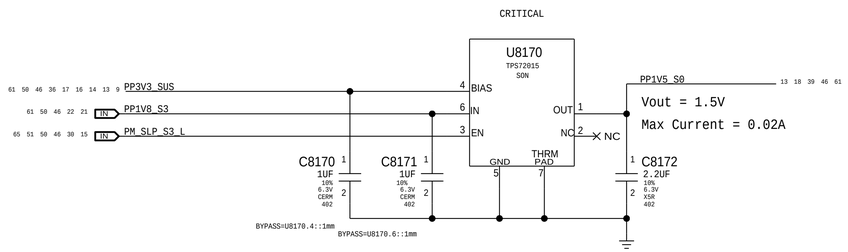
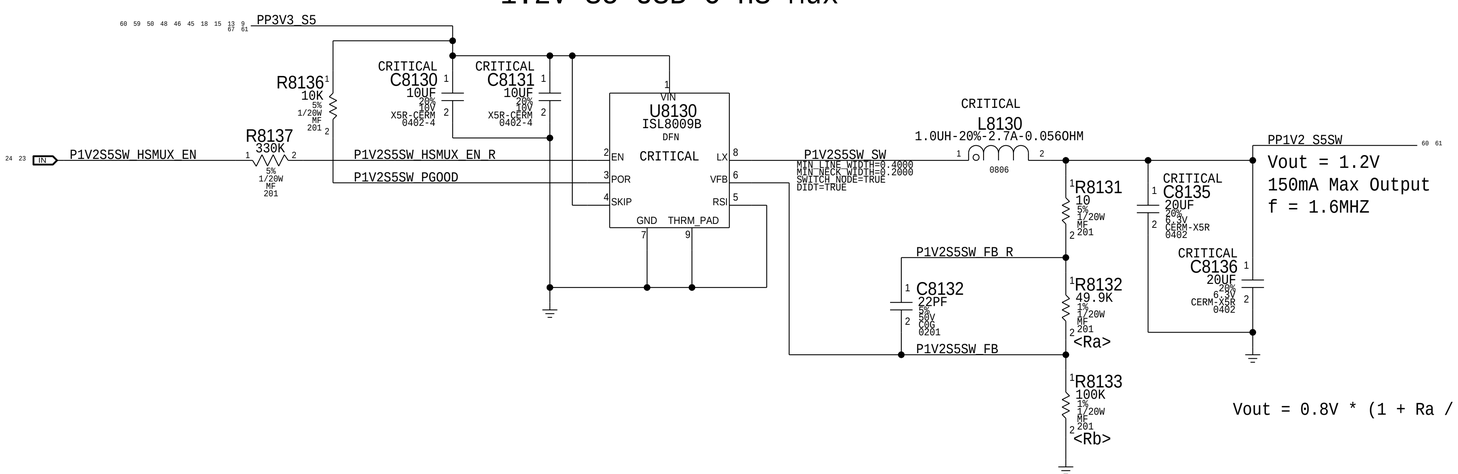
1.5V S0 LDO



1.2V S5 USB-C HS Mux



Vout = 0.8V * (1 + Ra / Rb)

SYNC_MASTER=X260_ERIC SYNC_DATE=06/15/2015

PAGE TITLE

Misc Power Supplies

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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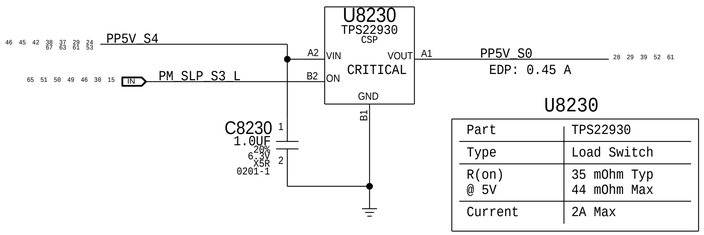
5V S0 Switch

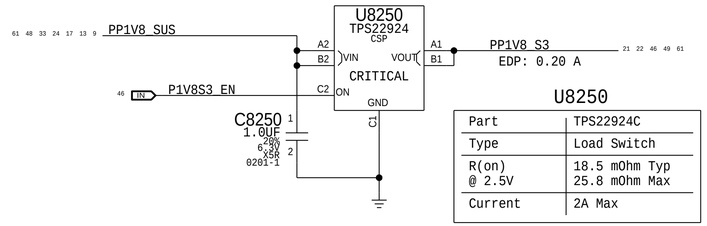


U8230

Part	TPS22930
Type	Load Switch
R(on) @ 5V	35 mOhm Typ 44 mOhm Max
Current	2A Max

1.8V S3 Switch

(LPDDR3)

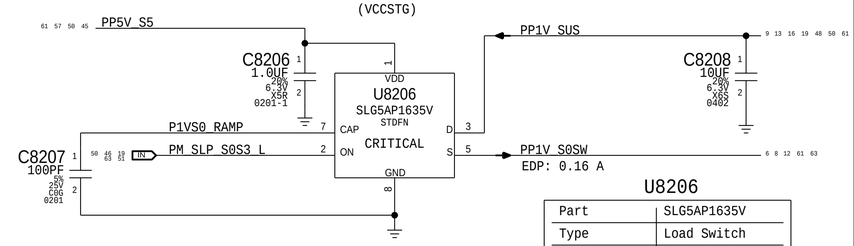


U8250

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

1.0V S0SW Switch

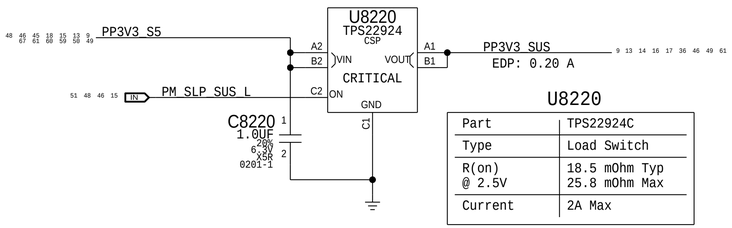
(VCCSTG)



U8206

Part	SLG5AP1635V
Type	Load Switch
R(on) @ 4V Vgs	20 mOhm Typ 28 mOhm Max
Current	2.5A Max

3.3V SUS Switch



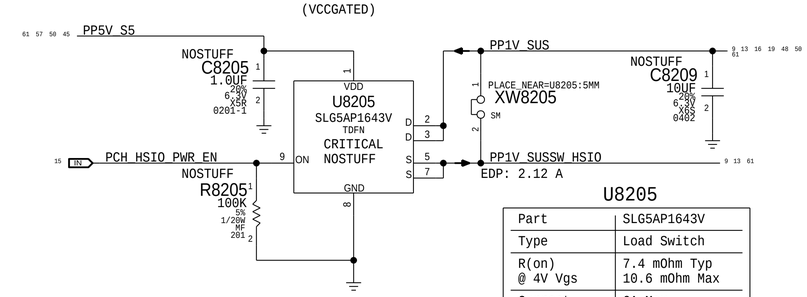
U8220

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

HSIO FET de-featured from SKL
leaving placeholder for CNL

1.0V SUSSW HSIO Switch

(VCCGATED)

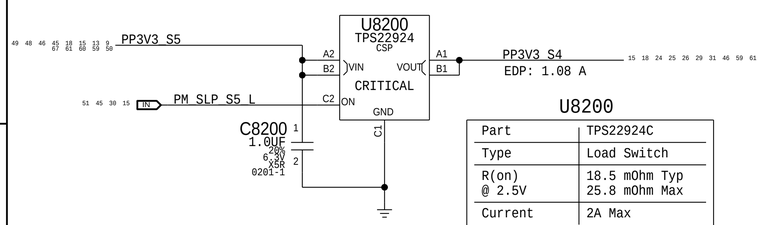


HSIO has turn-on requirement of
10uS min and 200uS max
from EN to 0.95V

U8205

Part	SLG5AP1643V
Type	Load Switch
R(on) @ 4V Vgs	7.4 mOhm Typ 10.6 mOhm Max
Current	6A Max

3.3V S4 Switch

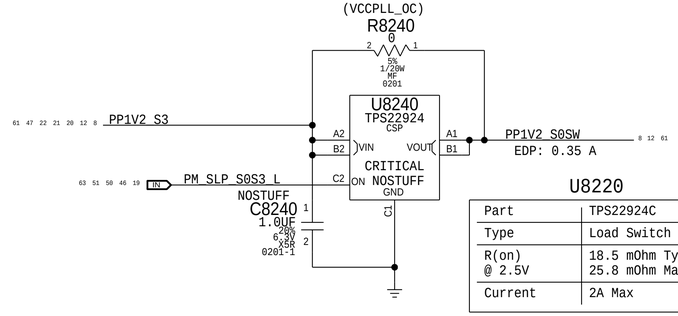


U8200

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

1.2V S0SW Switch

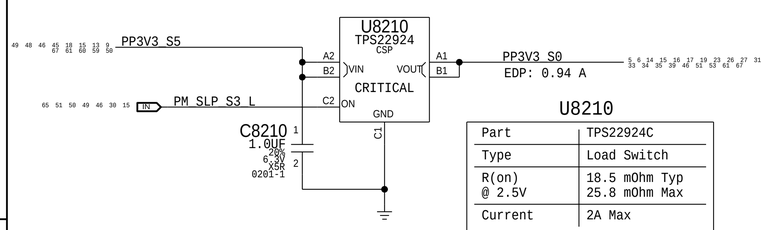
(VCCPLL_OC)



U8220

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

3.3V S0 Switch

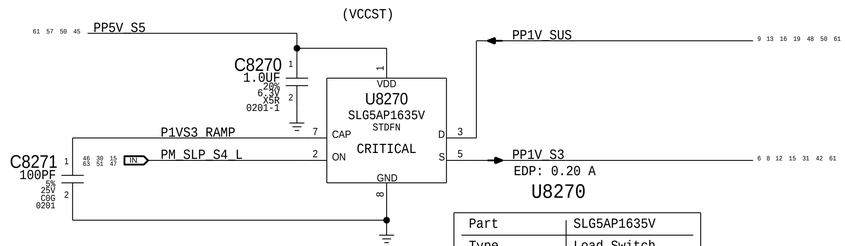


U8210

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

1.0V S3 Switch

(VCCST)



U8270

Part	SLG5AP1635V
Type	Load Switch
R(on) @ 4V Vgs	20 mOhm Typ 28 mOhm Max
Current	2.5A Max

SYNC_MASTER=DEVMLB SYNC_DATE=05/06/2015

PAGE TITLE

Power FETs

Apple Inc.

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REVISION <E4LABEL>

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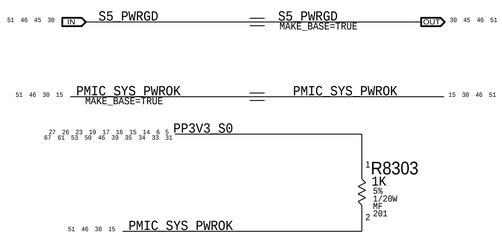
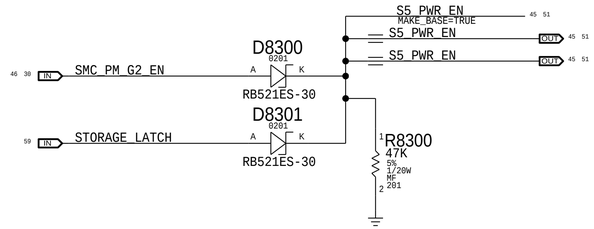
Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	PM_SUS_EN	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	0
Deep Sleep (S4)	0	1	0	1	0	0
Deep Sleep (S5)	0	1	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0

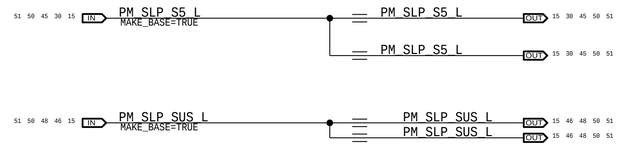
S5 Power Good (3.3V DSW PGOOD based)



S5 Enables

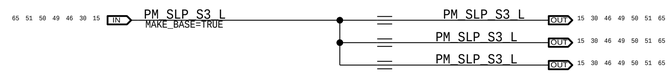


SUS & S4 Enables

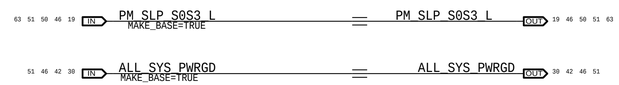


S3 Enables

S0 Enables



S0I Enables



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Power Control

Apple Inc.

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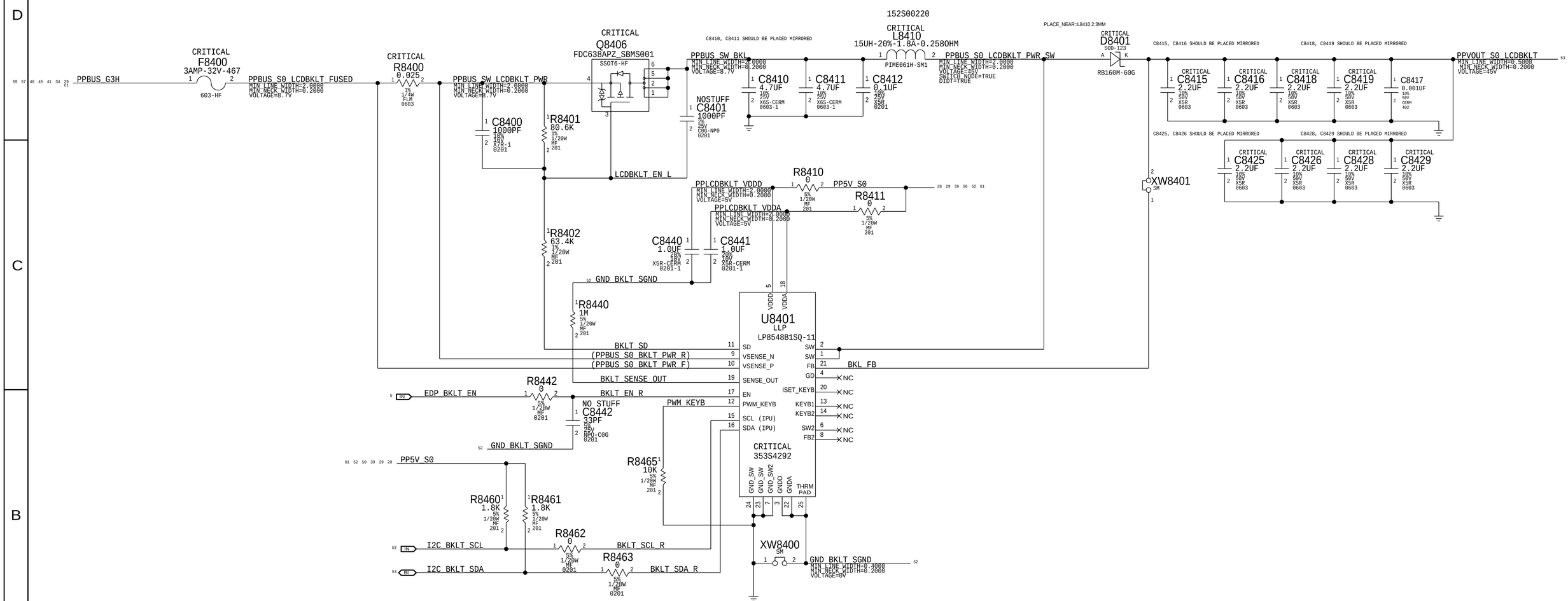

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LCD Backlight Driver

Apple Inc.

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SIZE	D
REVISION	<E4LABEL>
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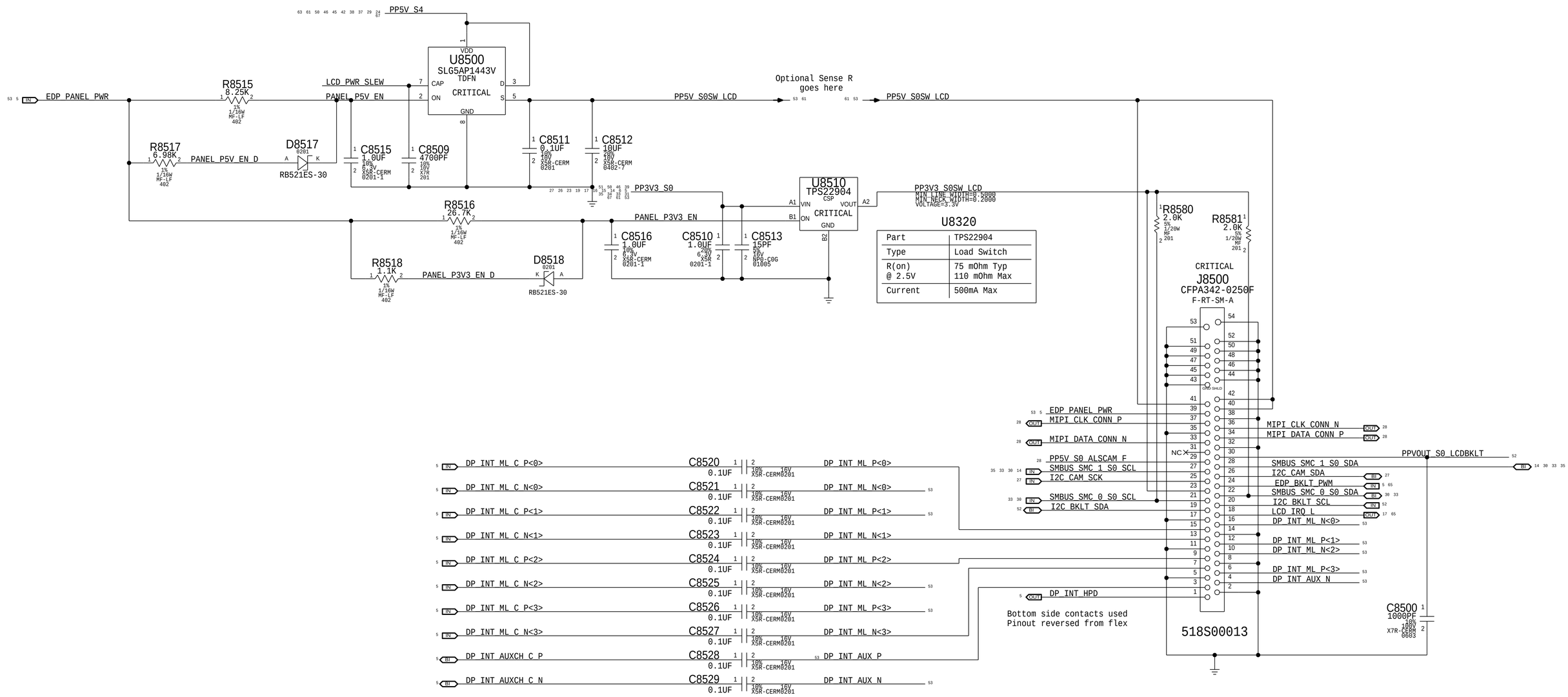
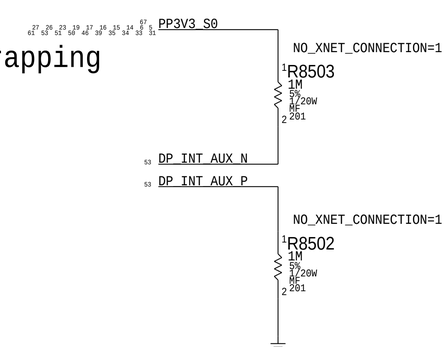
LCD PANEL INTERFACE (eDP) + Camera (MIPI)



LCD Panel HPD & AUX strapping



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PAGE TITLE: eDP Display Connector

Apple Inc.

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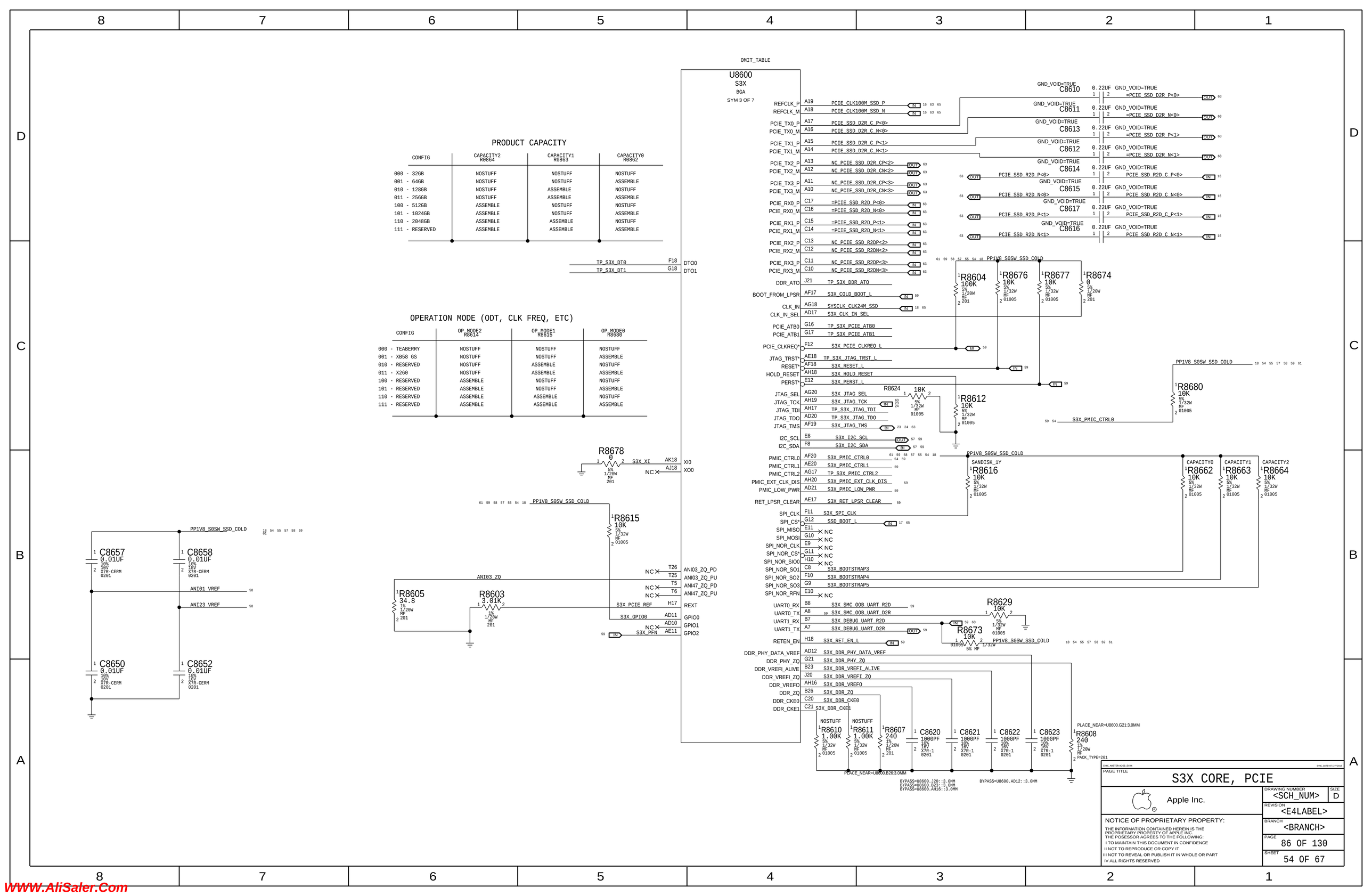

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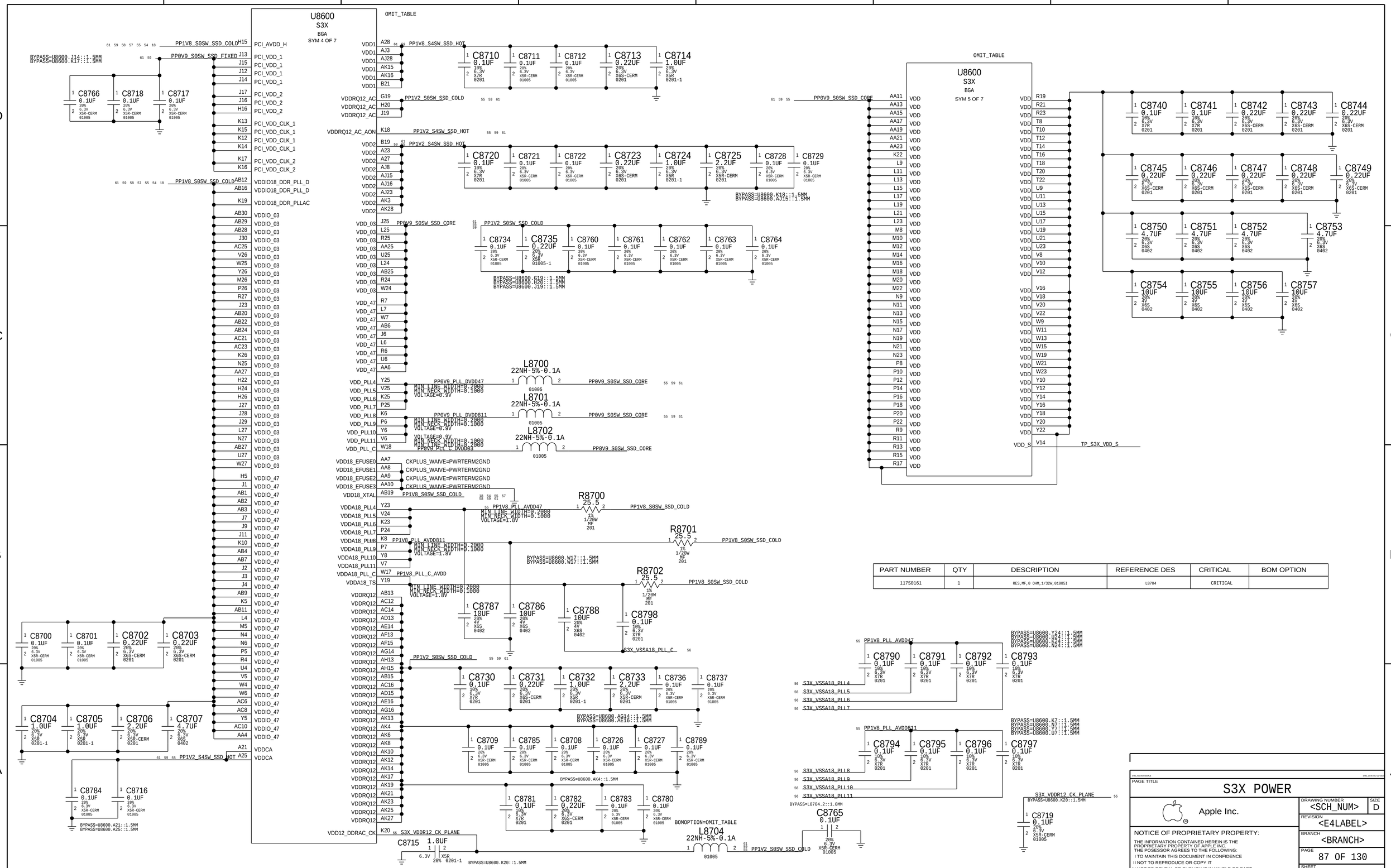
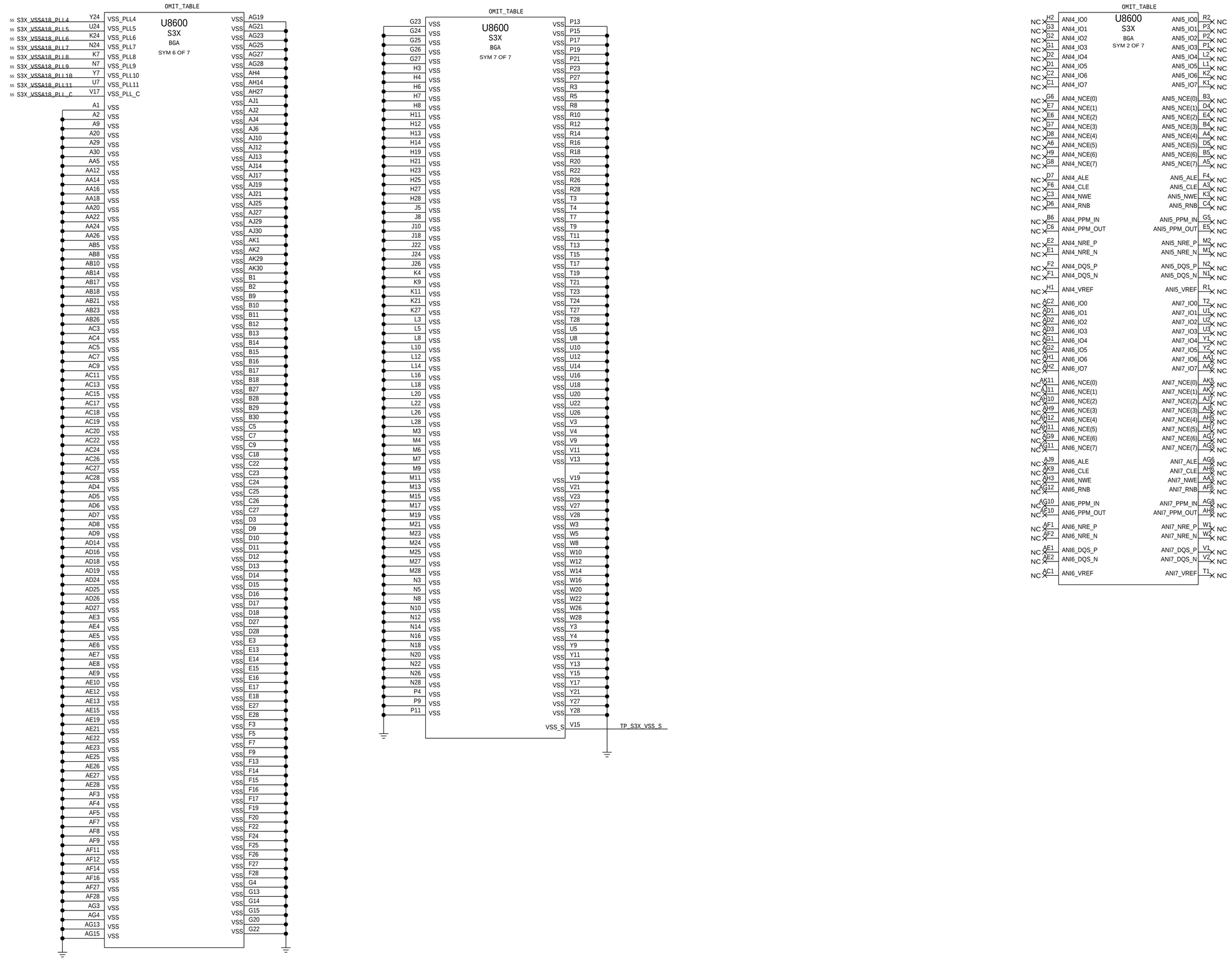


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0161	1	RES,MF,0 OHM,1/32W,01005I	L8704	CRITICAL	



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PAGE TITLE

S3X GND

Apple Inc.

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DEVICE 2-WIRE ADDRESS	ADD0 PIN CONNECTION
1001010	SDA

PLACE U9010 Opposite of S3X controller

61 59 58 55 54 18 PP1V8_S0SW_SSD_COLD

R9010 4.7K 5% 1/20W MF 201

R9011 4.7K 5% 1/20W MF 201

U9010 HPA00330AI SOT563

V+ (5) · SDA (6) · SCL (1) · ADD0 (4) · ALERT (3) · GND (2)

59 57 54 BI S3X_I2C_SDA

59 54 BI S3X_I2C_SCL

S3X_I2C_SDA · NC

C9010 0.01UF 10% 10V X5R-CERM 0201 — BYPASS=U9010.5::3.0MM

61 59 58 57 PP3V3R2V7_NAND_VCC

R9003 10K 1% 1/20W MF 201 — NO_XNET_CONNECTION=1

R9031 10K 0.1% 1/20W MF 0201-1 — NO_XNET_CONNECTION=1

61 50 45 PP5V_S5

R9001 2.2 5% 1/20W MF 201

R9006 2.2 5% 1/20W MF 201

PP2V7_NAND_PVCC — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.2000, VOLTAGE=5V

C9021 10UF 20% 6.3V CERM-X6S 0402

PP2V7_NAND_VCC — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.2000, VOLTAGE=5V

C9022 2.2UF 10% 10V X6S-CERM 0402

61 59 52 46 45 41 34 29 PPBUS_G3H

P2V7NAND_BOOT_RC — MIN_LINE_WIDTH=0.3000, MIN_NECK_WIDTH=0.2000, DIDT=TRUE

C9016 0.1UF 10% 16V X7R-CERM 0402

R9009 2.2 5% 1/20W MF 201

P2V7NAND_VBST — MIN_LINE_WIDTH=0.3000, MIN_NECK_WIDTH=0.2000, DIDT=TRUE

P2V7NAND_DRVH_R — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.2000, GATE_NODE=TRUE, DIDT=TRUE

R9039 0 5% 1/20W MF 0201

P2V7NAND_DRVH — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.2000, GATE_NODE=TRUE, DIDT=TRUE

P2V7NAND_LL — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.2000, SWITCH_NODE=TRUE, DIDT=TRUE

65 P2V7NAND_DRVL — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.2000, GATE_NODE=TRUE, DIDT=TRUE

U9000 ISL95870AH UTQFN CRITICAL

Pin	Signal
15	EN
10	FB
7	SREF
12	VO
11	OCSET
14	PGOOD
4	RTN
13	FSEL
8	SET0
9	SET1
6	VID0
5	VID1
19	VCC
20	PVCC
18	BOOT
17	UGATE
16	PHASE
1	LGATE
3	GND
2	PGND

59 IN PICCOLO_VEN1

P2V7NAND_SENSE_DIV

P2V7NAND_SREF

P2V7NAND_VO

P2V7NAND_OCSET

59 OUT PICCOLO_POK1

P2V7NAND_RTN_DIV

P2V7NAND_SET0

P2V7NAND_SET1

C9023 0.01UF 10% 10V X7R-CERM 0201

R9017 191K 0.1% 1/20W MF 0201

R9018 95.3K 0.1% 1/20W MF 0201

P2V7NAND_SET_R

R9000 7.5K 1% 1/20W MF 201

C9026 10PF 5% 50V C0G 0201

R9004 10K 1% 1/20W MF 201

R9002 10K 0.1% 1/20W MF 0201-1

C9015 10PF 5% 50V C0G 0201

P2V7NAND_AGND — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.2000, VOLTAGE=0V

XW9000 SM — PLACE_NEAR=U9000.3:1mm

C9003 33UF 20% 16V TANT CASE-B1S

C9002 33UF 20% 16V TANT CASE-B1S

C9000 2.2UF 20% 25V X5R-CERM 0402-1

C9001 2.2UF 20% 25V X5R-CERM 0402-1

CRITICAL Q9001 CSD58879Q3D Q3D

VIN (1) · TG (3) · TGR (4) · VSW (6, 7, 8) · BG (5) · PGND (9)

P2V7NAND_SW_LL — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.2000, SWITCH_NODE=TRUE, DIDT=TRUE

CRITICAL L9000 0.68UH-20%-6.7A-0.01940HM PIMS042T-SM

P2V7NAND_R — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.2000, VOLTAGE=2.7V

CRITICAL R9030 0.003 1% 1/2W MF 0306

PP3V3R2V7_NAND_VCC 57 58 59 61

C9005 10UF 20% 16V X5R-CERM 0402-1

C9006 10UF 20% 16V X5R-CERM 0402-1

C9008 150UF 20% 6.3V POLY-TANT CASE-B3-SM

C9007 150UF 20% 6.3V POLY-TANT CASE-B3-SM

C9004 12PF 5% 25V NP0-C0G 0201

C9009 12PF 5% 25V NP0-C0G 0201

C9011 12PF 5% 25V NP0-C0G 0201

C9012 12PF 5% 25V NP0-C0G 0201

P2V7NAND_P

P2V7NAND_N

R9021 1.87K 1% 1/20W MF 201

NO_XNET_CONNECTION=1

C9070 2200PF 10% 25V CER-X7R 0201

R9072 1.87K 1% 1/20W MF 201

Vout = 2.85V
Freq = 1 MHz
Max OCP = 6.54 A
Nom OCP = 5.3 A
Min OCP = 4.1 A

SYNC_MASTER=X260_KUMAR — SYNC_DATE=06/16/2015

PAGE TITLE: NAND VR, I2C ROM, TEMP SENSORS

Apple Inc.

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REVISION: <E4LABEL>

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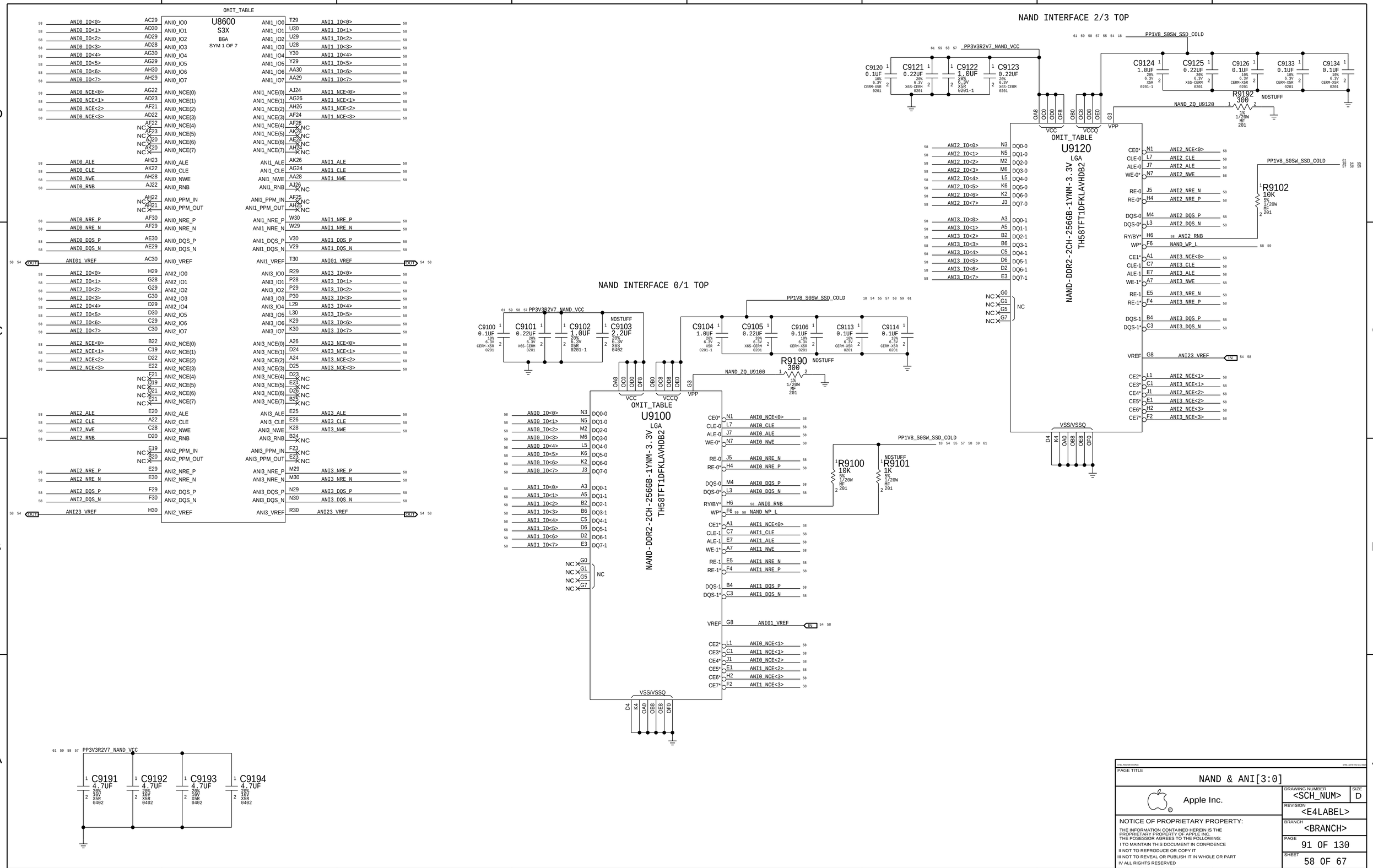

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NAND & ANI[3:0]

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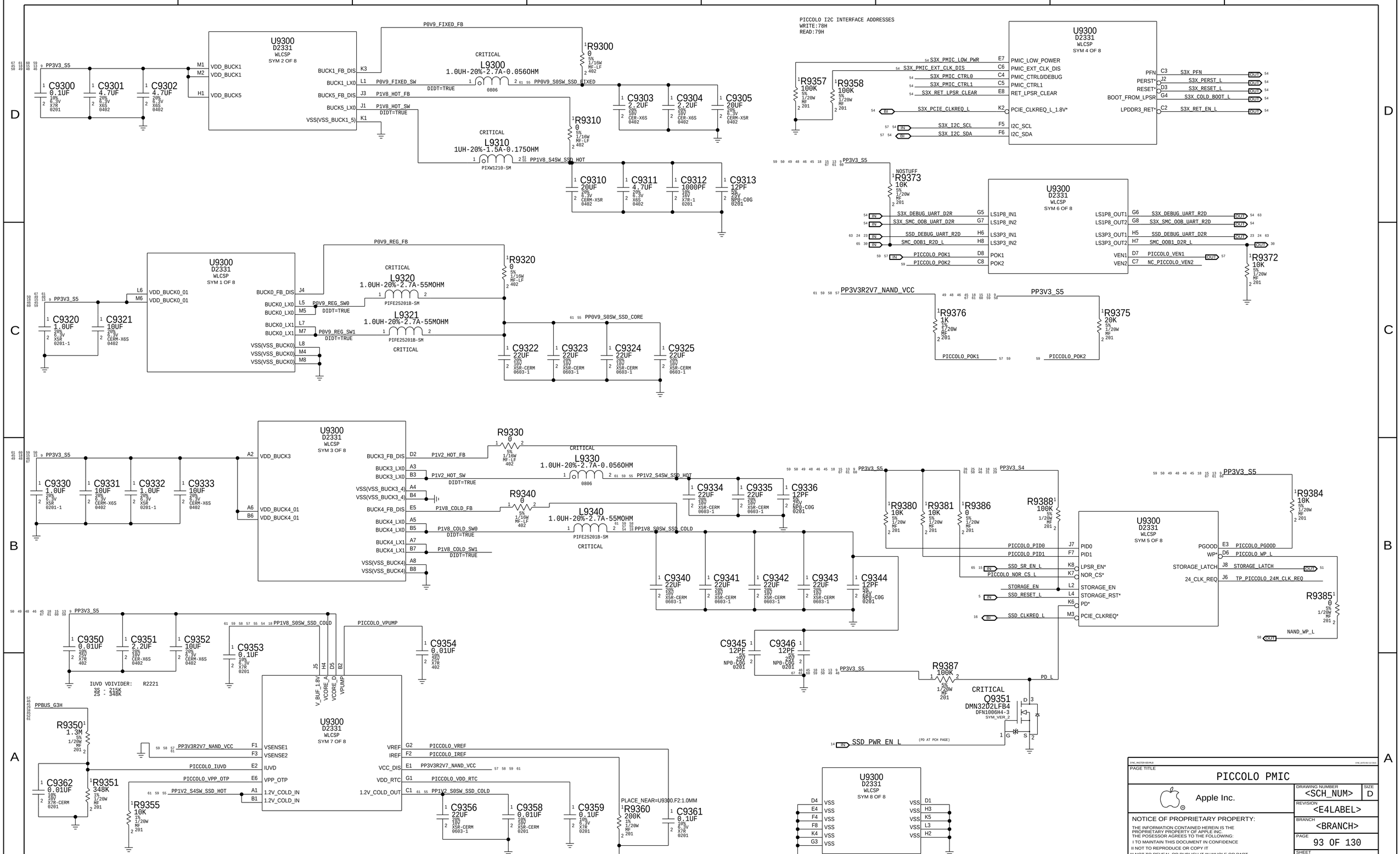
U9300 D2331 WLCSP SYM 2 OF 8
U9300 D2331 WLCSP SYM 4 OF 8
U9300 D2331 WLCSP SYM 6 OF 8
U9300 D2331 WLCSP SYM 1 OF 8
U9300 D2331 WLCSP SYM 3 OF 8
U9300 D2331 WLCSP SYM 5 OF 8
U9300 D2331 WLCSP SYM 7 OF 8
U9300 D2331 WLCSP SYM 8 OF 8
PICCOLO I2C INTERFACE ADDRESSES
WRITE:78H
READ:79H
PP3V3_S5
PP3V3_S4
PP3V3R2V7_NAND_VCC
PP0V9_FIXED_FB
PP0V9_S0SW_SSD_FIXED
PP1V8_S4SW_SSD_HOT
PP0V9_REG_FB
PP0V9_S0SW_SSD_CORE
PP1V2_HOT_FB
PP1V2_S4SW_SSD_HOT
PP1V8_S0SW_SSD_COLD
PICCOLO_VPUMP
PPBUS_G3H
PICCOLO_VREF
PICCOLO_IREF
PICCOLO_VDD_RTC
PICCOLO_IUVD
PICCOLO_VPP_OTP
PICCOLO_POK1
PICCOLO_POK2
PICCOLO_VEN1
NC_PICCOLO_VEN2
S3X_PMIC_LOW_PWR
S3X_PMIC_EXT_CLK_DIS
S3X_PMIC_CTRL0
S3X_PMIC_CTRL1
S3X_RET_LPSR_CLEAR
S3X_PCIE_CLKREQ_L
S3X_I2C_SCL
S3X_I2C_SDA
S3X_PFN
S3X_PERST_L
S3X_RESET_L
S3X_COLD_BOOT_L
S3X_RET_EN_L
S3X_DEBUG_UART_D2R
S3X_SMC_OOB_UART_D2R
SSD_DEBUG_UART_R2D
SMC_OOB1_R2D_L
S3X_DEBUG_UART_R2D
S3X_SMC_OOB_UART_R2D
SSD_DEBUG_UART_D2R
SMC_OOB1_R2D_L
SSD_PWR_EN_L
(PD AT PCH PAGE)
SSD_RESET_L
SSD_CLKREQ_L
PCIE_CLKREQ*
PCICLO_PID0
PCICLO_PID1
SSD_SR_EN_L
PICCOLO_NOR_CS_L
STORAGE_EN
STORAGE_RST*
PD*
PD_L
PICCOLO_PGOOD
PICCOLO_WP_L
STORAGE_LATCH
TP_PICCOLO_24M_CLK_REQ
NAND_WP_L
CRITICAL
L9300 1.0UH-20%-2.7A-0.0560HM
L9310 1UH-20%-1.5A-0.1750HM
L9320 1.0UH-20%-2.7A-55MOHM
L9321 1.0UH-20%-2.7A-55MOHM
L9330 1.0UH-20%-2.7A-0.0560HM
L9340 1.0UH-20%-2.7A-55MOHM
Q9351 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2
IUVD VDIVIDER: R2221
3S - 215K
2S - 348K
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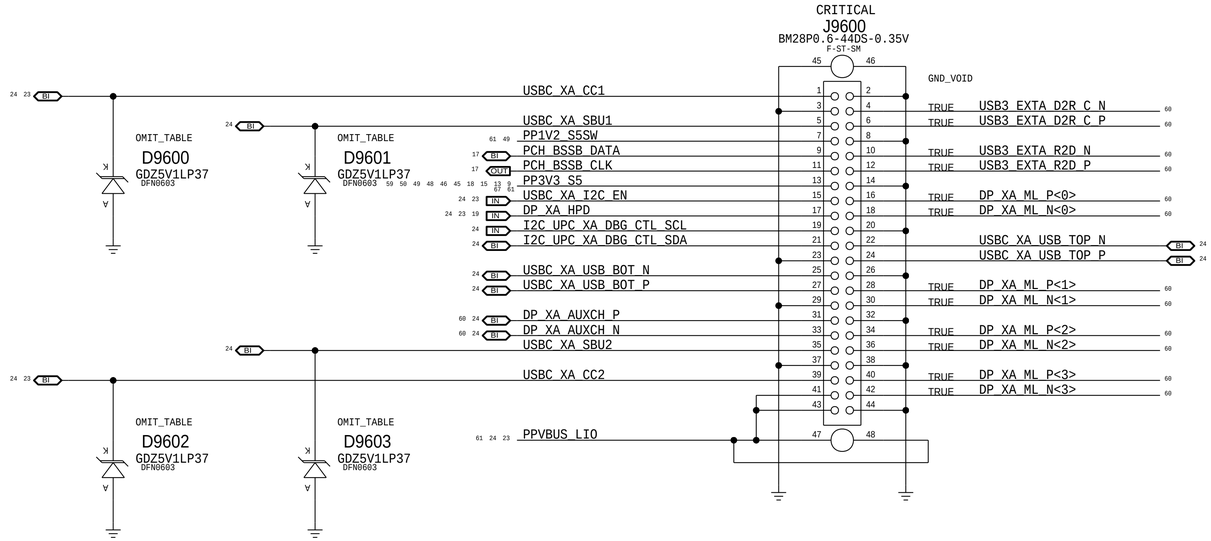
USB-C B2B RECEPTACLE
516S00038



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
371S00075	4	DIODE,ZENER,6.2V,250MW,DFN0603	D9600,D9601,D9602,D9603	CRITICAL	

USB3 AC COUPLING

GND_VOID=TRUE (ALL CAPS)

USB3_EXTA_D2R_P	C9620 0.1UF	USB3_EXTA_D2R_C_P	10% 16V 0201 X5R-CERM
USB3_EXTA_D2R_N	C9621 0.1UF	USB3_EXTA_D2R_C_N	10% 16V 0201 X5R-CERM
USB3_EXTA_R2D_C_P	C9622 0.1UF	USB3_EXTA_R2D_P	10% 16V 0201 X5R-CERM
USB3_EXTA_R2D_C_N	C9623 0.1UF	USB3_EXTA_R2D_N	10% 16V 0201 X5R-CERM

DP SNK0 AC COUPLING

GND_VOID=TRUE (ALL CAPS)

DP_XA_ML_C_P<0>	C9630 0.1UF	DP_XA_ML_P<0>	10% 16V 0201 X5R-CERM
DP_XA_ML_C_N<0>	C9631 0.1UF	DP_XA_ML_N<0>	10% 16V 0201 X5R-CERM
DP_XA_ML_C_P<1>	C9632 0.1UF	DP_XA_ML_P<1>	10% 16V 0201 X5R-CERM
DP_XA_ML_C_N<1>	C9633 0.1UF	DP_XA_ML_N<1>	10% 16V 0201 X5R-CERM
DP_XA_ML_C_P<2>	C9634 0.1UF	DP_XA_ML_P<2>	10% 16V 0201 X5R-CERM
DP_XA_ML_C_N<2>	C9635 0.1UF	DP_XA_ML_N<2>	10% 16V 0201 X5R-CERM
DP_XA_ML_C_P<3>	C9636 0.1UF	DP_XA_ML_P<3>	10% 16V 0201 X5R-CERM
DP_XA_ML_C_N<3>	C9637 0.1UF	DP_XA_ML_N<3>	10% 16V 0201 X5R-CERM
DP_XA_AUXCH_C_P	C9638 0.1UF	DP_XA_AUXCH_P	10% 16V 0201 X5R-CERM
DP_XA_AUXCH_C_N	C9639 0.1UF	DP_XA_AUXCH_N	10% 16V 0201 X5R-CERM

SYNC_MASTER=DEVMLB SYNC_DATE=03/16/2015

PAGE TITLE
LIO Flex Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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"G3Hot" (Always-Present) Rails

PPBUS_G3H
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=8.6V
MAKE_BASE=TRUE

PPVIN_G3H_P3V3G3H
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=8.6V
MAKE_BASE=TRUE

PPBUS_S5_HS_COMPUTING_ISNS
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=8.6V
MAKE_BASE=TRUE

PPVBUS_LIO
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1000
VOLTAGE=20V
MAKE_BASE=TRUE

PPDCIN_G3H
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=20V
MAKE_BASE=TRUE

PP3V3_G3H
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.2000
VOLTAGE=3.42V
MAKE_BASE=TRUE

PP3V3R3V0_AON
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1000
VOLTAGE=3.3V
MAKE_BASE=TRUE

PPVRTC_G3H
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=3V
MAKE_BASE=TRUE

5V Rails

PP5V_G3H
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.2000
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S5
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.2000
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S0SW_LCD
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.2000
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S4
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.2000
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S0
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.2000
VOLTAGE=5V
MAKE_BASE=TRUE

3.3V Rails

PP3V3_S5
MIN_LINE_WIDTH=0.6000 VOLTAGE=3.3V
MIN_NECK_WIDTH=0.1000 MAKE_BASE=TRUE

PP3V3_SUS
MIN_LINE_WIDTH=0.6000 VOLTAGE=3.3V
MIN_NECK_WIDTH=0.1000 MAKE_BASE=TRUE

PP3V3_S4
MIN_LINE_WIDTH=0.6000 VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2000 MAKE_BASE=TRUE

PP3V3_S0
MIN_LINE_WIDTH=0.6000 VOLTAGE=3.3V
MIN_NECK_WIDTH=0.1000 MAKE_BASE=TRUE

1.8V Rails

PP1V8_SUS
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.8V
MAKE_BASE=TRUE

PP1V8_S3
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.8V
MAKE_BASE=TRUE

PP1V5_S0
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.5V
MAKE_BASE=TRUE

1.2V Rails

PP1V2_S3
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1500
VOLTAGE=1.2V
MAKE_BASE=TRUE

PP1V2_S0SW
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1000
VOLTAGE=1.2V
MAKE_BASE=TRUE

PP1V2_S5SW
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1000
VOLTAGE=1.2V
MAKE_BASE=TRUE

Chipset Rails

PP1V_SUS
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.0V
MAKE_BASE=TRUE

PP1V_SUSSW_HSIO
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.0V
MAKE_BASE=TRUE

PP1V_S3
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.0V
MAKE_BASE=TRUE

PP1V_S0SW
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.0V
MAKE_BASE=TRUE

PPVCCIO_S0
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2500
VOLTAGE=1.0V
MAKE_BASE=TRUE

PPVCCSA_S0
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.0V
MAKE_BASE=TRUE

PPVCCSA_DDR_S0
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.0V
MAKE_BASE=TRUE

SSD Rails

PP3V3R2V7_NAND_VCC
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1000
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP1V8_S0SW_SSD_COLD
MIN_LINE_WIDTH=0.9950
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.8V
MAKE_BASE=TRUE

PP1V2_S0SW_SSD_COLD
MIN_LINE_WIDTH=0.9950
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.2V
MAKE_BASE=TRUE

PP1V8_S4SW_SSD_HOT
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.8V
MAKE_BASE=TRUE

PP1V2_S4SW_SSD_HOT
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.2V
MAKE_BASE=TRUE

PP0V9_S0SW_SSD_CORE
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1500
VOLTAGE=0.9V
MAKE_BASE=TRUE

PP0V9_S0SW_SSD_FIXED
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1500
VOLTAGE=0.9V
MAKE_BASE=TRUE

CPU "VCORE" RAILS

PPVCORE_S0_CPU
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1000
VOLTAGE=1.8V
MAKE_BASE=TRUE

GT "VCORE" RAILS

PPVCORE_S0_GT
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1000
VOLTAGE=1.8V
MAKE_BASE=TRUE

PCH "VCORE" RAILS

PPVCORE_SUS_PCH
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1000
VOLTAGE=1.8V
MAKE_BASE=TRUE

PP5V_S4RS0
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.2000
VOLTAGE=5V
MAKE_BASE=TRUE

RA000 0 2 1 5% 1/20W MF 0201
RA001 0 2 1 5% 1/20W MF 0201
NO STUFF

? mA

Digital Ground

GND
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=0V

SYNC_MASTER=X260_ERIC SYNC_DATE=06/09/2015

PAGE TITLE
Power Aliases

Apple Inc.

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Memory Bit/Byte Swizzle

	MAKE_BASE		
MEM A DQ<39>	TRUE	MEM A DQ<39>	62 21 7 BI 7 21 62
MEM A DQ<37>	TRUE	MEM A DQ<37>	62 21 7 BI 7 21 62
MEM A DQ<33>	TRUE	MEM A DQ<33>	62 21 7 BI 7 21 62
MEM A DQ<36>	TRUE	MEM A DQ<36>	62 21 7 BI 7 21 62
MEM A DQ<38>	TRUE	MEM A DQ<38>	62 21 7 BI 7 21 62
MEM A DQ<34>	TRUE	MEM A DQ<34>	62 21 7 BI 7 21 62
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MEM A DQ<42>	TRUE	MEM A DQ<42>	62 21 7 BI 7 21 62
MEM A DQ<41>	TRUE	MEM A DQ<41>	62 21 7 BI 7 21 62
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	MAKE_BASE		
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SYNC_MASTER=DEVMLB SYNC_DATE=04/30/2015

PAGE TITLE
Memory Signal Swaps

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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63 46 42	CPU_VR_READY	TRUE	CPU_VR_READY	42 46 63	MAKE_BASE
63 30 15	SMC_PCH_SUSWARN_L	TRUE	SMC_PCH_SUSWARN_L	15 30 63	
63 30 15	SMC_PCH_SUSACK_L	TRUE	SMC_PCH_SUSACK_L	15 30 63	
63 41 34 31 30 65	SMC_BC_ACOK	TRUE	SMC_BC_ACOK	30 31 34 41 63 65	
65 24 23 16	XDP_USB_EXTA_OC_L	TRUE	USB_EXTA_OC_L	23	
64 63 16	USB_EXTB_OC_L	TRUE	USB_EXTB_OC_L	16 63 64	
63 46 30 15	PM_RSMRST_L	TRUE	PM_RSMRST_L	15 30 46 63	
	GND	TRUE	GND		MAKE_BASE
63 46 45	P5VS4_PGOOD	TRUE	P5VS4_PGOOD	45 46 63	
42 38 37 29 53 63 50 46 45	PP5V_S4	TRUE	PP5V_S4	24 29 37 38 42 45 46 50 53 61 63 67	
54	=PCIE_SSD_R2D_P<1..0>	TRUE	PCIE_SSD_R2D_P<1..0>	54	
54	=PCIE_SSD_R2D_N<1..0>	TRUE	PCIE_SSD_R2D_N<1..0>	54	
	=PCIE_SSD_R2D_P<3..2>	TRUE 1	NC_PCIE_SSD_R2DP<3..2>	54	
	=PCIE_SSD_R2D_N<3..2>	TRUE 1	NC_PCIE_SSD_R2DN<3..2>	54	
	PCIE_SSD_R2D_C_P<3..2>	TRUE 1	NC_PCIE_SSD_R2D_CP<3..2>	16	
	PCIE_SSD_R2D_C_N<3..2>	TRUE 1	NC_PCIE_SSD_R2D_CN<3..2>	16	
54	=PCIE_SSD_D2R_P<1..0>	TRUE	PCIE_SSD_D2R_P<1..0>	16 65	
54	=PCIE_SSD_D2R_N<1..0>	TRUE	PCIE_SSD_D2R_N<1..0>	16 65	
	PCIE_SSD_D2R_C_P<3..2>	TRUE 1	NC_PCIE_SSD_D2R_CP<3..2>	54	
	PCIE_SSD_D2R_C_N<3..2>	TRUE 1	NC_PCIE_SSD_D2R_CN<3..2>	54	
	PCIE_SSD_D2R_P<3..2>	TRUE 1	NC_PCIE_SSD_D2RP<3..2>	16	
	PCIE_SSD_D2R_N<3..2>	TRUE 1	NC_PCIE_SSD_D2RN<3..2>	16	
65 63 54 16	PCIE_CLK100M_SSD_P	TRUE	PCIE_CLK100M_SSD_P	16 54 63 65	
65 63 54 16	PCIE_CLK100M_SSD_N	TRUE	PCIE_CLK100M_SSD_N	16 54 63 65	
63 59 54	S3X_DEBUG_UART_R2D	TRUE	S3X_DEBUG_UART_R2D	54 59 63	
59 24 23	SSD_DEBUG_UART_D2R	TRUE	SSD_UART_D2R	17 65	
59 24 23	SSD_DEBUG_UART_R2D	TRUE	SSD_UART_R2D	17 65	
63 51 50 46 19	PM_SLP_S0S3_L	TRUE	PM_SLP_S0S3_L	19 46 50 51 63	
50 47 46 30 15 63 51	PM_SLP_S4_L	TRUE	PM_SLP_S4_L	15 30 46 47 50 51 63	
65 63 18 16	SYSCLK_CLK24M_PCH	TRUE	SYSCLK_CLK24M_PCH	16 18 63 65	
63 16	NC_PCH_CLK24M_XTALOUT	TRUE	NC_PCH_CLK24M_XTALOUT	16 63	
63 5	NC_PCH_DDPC_CTRLDATA	TRUE	NC_PCH_DDPC_CTRLDATA	5 63	

63 6	NC_CPU_CFG0	TRUE	NC_CPU_CFG0	6 63	MAKE_BASE
63 6	NC_CPU_CFG1	TRUE	NC_CPU_CFG1	6 63	
63 6	NC_CPU_CFG2	TRUE	NC_CPU_CFG2	6 63	
63 6	TP_CPU_CFG3	TRUE	TP_CPU_CFG3	6 63	
63 6	NC_CPU_CFG5	TRUE	NC_CPU_CFG5	6 63	
63 6	NC_CPU_CFG6	TRUE	NC_CPU_CFG6	6 63	
63 6	NC_CPU_CFG7	TRUE	NC_CPU_CFG7	6 63	
63 6	NC_CPU_CFG8	TRUE	NC_CPU_CFG8	6 63	
63 6	NC_CPU_CFG9	TRUE	NC_CPU_CFG9	6 63	
63 6	NC_CPU_CFG10	TRUE	NC_CPU_CFG10	6 63	
63 6	NC_CPU_CFG11	TRUE	NC_CPU_CFG11	6 63	
63 6	NC_CPU_CFG12	TRUE	NC_CPU_CFG12	6 63	
63 6	NC_CPU_CFG13	TRUE	NC_CPU_CFG13	6 63	
63 6	NC_CPU_CFG14	TRUE	NC_CPU_CFG14	6 63	
63 6	NC_CPU_CFG15	TRUE	NC_CPU_CFG15	6 63	
63 6	NC_CPU_CFG16	TRUE	NC_CPU_CFG16	6 63	
63 6	NC_CPU_CFG17	TRUE	NC_CPU_CFG17	6 63	
63 6	NC_CPU_CFG18	TRUE	NC_CPU_CFG18	6 63	
63 6	NC_CPU_CFG19	TRUE	NC_CPU_CFG19	6 63	
	XDP_BPM_L<3..0>	TRUE	TP_XDP_BPM_L<3..0>	6	
63 16	TP_XDP_CPU_PRDY_L	TRUE	TP_XDP_CPU_PRDY_L	16 63	
63 16	TP_XDP_CPU_PREQ_L	TRUE	TP_XDP_CPU_PREQ_L	16 63	
63 6	XDP_CPUPCH_TCK	TRUE	XDP_CPUPCH_TCK	6 63	
63 6	XDP_CPUPCH_TDI	TRUE	XDP_CPUPCH_TDI	6 63	
63 6	XDP_CPUPCH_TDO	TRUE	63 6 XDP_CPUPCH_TDO		
63 6	XDP_CPUPCH_TMS	TRUE	XDP_CPUPCH_TMS	6 63	
63 6	XDP_CPUPCH_TRST_L	TRUE	XDP_CPUPCH_TRST_L	6 63	
63 16	TP_XDP_PCH_OBSDATA_A2	TRUE	TP_XDP_PCH_OBSDATA_A2	16 63	
63 6	TP_XDP_PCH_OBSDATA_A3	TRUE	TP_XDP_PCH_OBSDATA_A3	6 63	
63 16	TP_XDP_PCH_OBSDATA_B0	TRUE	TP_XDP_PCH_OBSDATA_B0	16 63	
63 14	TP_XDP_PCH_OBSDATA_C0	TRUE	TP_XDP_PCH_OBSDATA_C0	14 63	
63 14	TP_XDP_PCH_OBSDATA_C1	TRUE	TP_XDP_PCH_OBSDATA_C1	14 63	
63 14	TP_XDP_PCH_OBSDATA_C2	TRUE	TP_XDP_PCH_OBSDATA_C2	14 63	
63 14	TP_XDP_PCH_OBSDATA_C3	TRUE	TP_XDP_PCH_OBSDATA_C3	14 63	
63 14	TP_XDP_PCH_OBSDATA_D0	TRUE	TP_XDP_PCH_OBSDATA_D0	14 63	
63 16	TP_XDP_PCH_OBSDATA_D1	TRUE	TP_XDP_PCH_OBSDATA_D1	16 63	
63 16	TP_XDP_PCH_OBSDATA_D2	TRUE	TP_XDP_PCH_OBSDATA_D2	16 63	
63 16	TP_XDP_PCH_OBSDATA_D3	TRUE	TP_XDP_PCH_OBSDATA_D3	16 63	
63 6	TP_XDP_PCH_OBSFN_C1	TRUE	TP_XDP_PCH_OBSFN_C1	6 63	
63 6	TP_XDP_PCH_TCK	TRUE	TP_XDP_PCH_TCK	6 63	
63 6	XDP_CPUPCH_TDI	TRUE	XDP_CPUPCH_TDI	6 63	
63 6	XDP_CPUPCH_TDO	TRUE	XDP_CPUPCH_TDO	6 63	
63 6	XDP_CPUPCH_TMS	TRUE	XDP_CPUPCH_TMS	6 63	
63 6	XDP_CPUPCH_TRST_L	TRUE	XDP_CPUPCH_TRST_L	6 63	
63 6	XDP_CPUPCH_TCK	TRUE	63 6 XDP_CPUPCH_TCK		
63 6	TP_ITP_PMODE	TRUE	TP_ITP_PMODE	6 63	
63 7	TP_CPU_MEMVTT_PWR_EN	TRUE	TP_CPU_MEMVTT_PWR_EN	7 63	
63 30	TP_SMC_DEV_MLB	TRUE	TP_SMC_DEV_MLB	30 63	
54 24 23	S3X_JTAG_TCK	TRUE	TP_S3X_JTAG_TCK		
54 24 23	S3X_JTAG_TMS	TRUE	TP_S3X_JTAG_TMS		

61 50 12 8 6 PP1V_S0SW

RA300 51 1 2 5% 1/20W MF 201

RA301 51 1 2 5% 1/20W MF 201

63 30	TP_SMC_DEBUGPRT_EN_L	TRUE	TP_SMC_DEBUGPRT_EN_L	30 63
63 14	TP_SPKR_ID0	TRUE	TP_SPKR_ID0	14 63
63 14	TP_SPKR_ID1	TRUE	TP_SPKR_ID1	14 63

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X260 Signal Aliases

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NO_TEST Nets

NO_TEST

64 14	NC_PCH_BT_I2S_CLK	TRUE	NC_PCH_BT_I2S_CLK	14 64	CPU/PCH
64 14	NC_PCH_BT_I2S_D2R	TRUE	NC_PCH_BT_I2S_D2R	14 64	
64 14	NC_PCH_BT_I2S_R2D	TRUE	NC_PCH_BT_I2S_R2D	14 64	
64 14	NC_PCH_BT_I2S_SYNC	TRUE	NC_PCH_BT_I2S_SYNC	14 64	
64 14	NC_HDA_SDIN1	TRUE	NC_HDA_SDIN1	14 64	
64 15	NC_PCI_PME_L	TRUE	NC_PCI_PME_L	15 64	
64 14	NC_CLINK_CLK	TRUE	NC_CLINK_CLK	14 64	
64 14	NC_CLINK_DATA	TRUE	NC_CLINK_DATA	14 64	
64 14	NC_CLINK_RESET_L	TRUE	NC_CLINK_RESET_L	14 64	
64 5	NC_DP_DDI2_AUXCH_CP	TRUE	NC_DP_DDI2_AUXCH_CP	5 64	
64 5	NC_DP_DDI2_AUXCH_CN	TRUE	NC_DP_DDI2_AUXCH_CN	5 64	
64 5	NC_DP_DDI2_ML_CP<0>	TRUE	NC_DP_DDI2_ML_CP<0>	5 64	
64 5	NC_DP_DDI2_ML_CN<0>	TRUE	NC_DP_DDI2_ML_CN<0>	5 64	
64 5	NC_DP_DDI2_ML_CP<1>	TRUE	NC_DP_DDI2_ML_CP<1>	5 64	
64 5	NC_DP_DDI2_ML_CN<1>	TRUE	NC_DP_DDI2_ML_CN<1>	5 64	
64 5	NC_DP_DDI2_ML_CP<2>	TRUE	NC_DP_DDI2_ML_CP<2>	5 64	
64 5	NC_DP_DDI2_ML_CN<2>	TRUE	NC_DP_DDI2_ML_CN<2>	5 64	
64 5	NC_DP_DDI2_ML_CP<3>	TRUE	NC_DP_DDI2_ML_CP<3>	5 64	
64 5	NC_DP_DDI2_ML_CN<3>	TRUE	NC_DP_DDI2_ML_CN<3>	5 64	
64 30	NC_TCON_BKLT_PWM	TRUE	NC_TCON_BKLT_PWM	30 64	SMC
64 30	NC_SMC_GFX_OVERTEMP	TRUE	NC_SMC_GFX_OVERTEMP	30 64	
64 30	NC_SMC_GFX_THROTTLE_L	TRUE	NC_SMC_GFX_THROTTLE_L	30 64	
64 30	NC_SMC_GFX_SELF_THROTTLE	TRUE	NC_SMC_GFX_SELF_THROTTLE	30 64	
64 30	NC_SMC_FAN_0_CTL	TRUE	NC_SMC_FAN_0_CTL	30 64	
64 30	NC_SMC_FAN_0_TACH	TRUE	NC_SMC_FAN_0_TACH	30 64	
64 30	NC_SMC_FAN_1_CTL	TRUE	NC_SMC_FAN_1_CTL	30 64	
64 30	NC_SMC_FAN_1_TACH	TRUE	NC_SMC_FAN_1_TACH	30 64	
64 30	NC_SYS_ONEWIRE	TRUE	NC_SYS_ONEWIRE	30 64	
64 30	NC_SMC_SOC_POR	TRUE	NC_SMC_SOC_POR	30 64	
64 30	NC_SMC_DP_HPD_L	TRUE	NC_SMC_DP_HPD_L	30 64	
64 30	NC_SPI_SMC_CLK	TRUE	NC_SPI_SMC_CLK	30 64	
64 30	NC_SPI_SMC_CS_L	TRUE	NC_SPI_SMC_CS_L	30 64	
64 30	NC_SPI_SMC_MISO	TRUE	NC_SPI_SMC_MISO	30 64	
64 30	NC_SPI_SMC_MOSI	TRUE	NC_SPI_SMC_MOSI	30 64	
64 30	NC_SMC_ACTUATOR_ACTIVE_L	TRUE	NC_SMC_ACTUATOR_ACTIVE_L	30 64	
64 30	NC_WIFI_DEBUGPRT_R2D_L	TRUE	NC_WIFI_DEBUGPRT_R2D_L	30 64	
64 30	NC_WIFI_DEBUGPRT_D2R_L	TRUE	NC_WIFI_DEBUGPRT_D2R_L	30 64	

Unused nets with offpage

(Nets with offpages not used on this project)

	CAM_SENSOR_WAKE_L	27		CPUCORE_ISNS1_P	OUT 43
1893	JTAG_ISP_TDO	5		CPUCORE_ISNS1_N	OUT 43
1890	TBT_POC_RESET	5		CPUCORE_ISNS2_P	OUT 43
1889	LCD_PSR_EN	17		CPUCORE_ISNS2_N	OUT 43
1888	TBT_X_PLUG_EVENT_L	17		CPUSA_ISNS_P	OUT 43
1887	TBT_T_PLUG_EVENT_L	17		CPUSA_ISNS_N	OUT 43
1886	TBT_X_PCI_RESET_L	14		CPUGT_ISNS1_P	OUT 44
1885	TBT_T_PCI_RESET_L	14		CPUGT_ISNS1_N	OUT 44
1884	TBT_X_CIO_PWR_EN	14		CPUGT_ISNS2_P	OUT 44
1883	TBT_T_CIO_PWR_EN	14		CPUGT_ISNS2_N	OUT 44
1882	TBT_X_USB_PWR_EN	14		SOC_UART_D2R	OUT 17
1881	TBT_T_USB_PWR_EN	14		SOC_UART_R2D	OUT 17
1880	BT_PWRRST_L	6		SOC_UART_CTS_L	OUT 17
1879	BT_TIMESTAMP	6		SOC_UART_RTS_L	OUT 17
1878	PCH_SWD_IO	17		CPU_CFG<4>	OUT 6
1877	PCH_SWD_MUX_SEL	17		DP_DDI2_HPD	IN 5
1876	SOC_WAKE_L	17		XDP_USB_EXTC_OC_L	IN 16
1875	PCH_SWD_CLK	17		XDP_USB_EXTD_OC_L	IN 16
1874	USB_EXTB_OC_L	16 63		XDP_JTAG_ISP_TCK	OUT 16
17	OUT AUD_SPI_CS_L			XDP_JTAG_ISP_TDI	OUT 16
17	OUT AUD_SPI_CLK				
17	IN AUD_SPI_MISO				
17	OUT AUD_SPI_MOSI				

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EE Chaz Probe Points

PPA504	SMC_CBC_ON	30 41
PPA505	SMC_CHGR_INT_L	30 41
PPA506	MEM_A_CAA<0>	7 21
PPA507	MEM_A_CLK_P<0>	7 21
PPA508	MEM_A_CLK_N<0>	7 21
PPA509	MEM_A_CS_L<0>	7 21
PPA510	MEM_B_DQ<12>	7 22 62
PPA511	MEM_A_DQS_P<1>	7 21 62
PPA512	MEM_A_DQS_N<1>	7 21 62
PPA513	AP_DEV_WAKE	14 25
PPA514	AP_S0IX_WAKE_L	17 18
PPA515	AP_S0IX_WAKE_SEL	17 18
PPA517	MIPI_CLK_P	27 28
PPA518	MIPI_DATA_P	27 28
PPA519	PCH_BT_UART_D2R	17 26
PPA520	PCH_BT_UART_RTS_L	17 26
PPA522	PCIE_CAMERA_D2R_P	16 28
PPA523	PCIE_CLK100M_SSD_P	16 54 63
PPA529	AUD_PWR_EN	17 39
PPA530	BT_UART_RTS_L	25 26
PPA531	CAMERA_PWR_EN	14 27
PPA533	EDP_BKLT_PWM	5 53
PPA534	HDA_SDIN0	14 39
PPA537	LCD_IRQ_L	17 53
PPA538	MEM_CAM_A<8>	27 28
PPA539	MEM_CAM_CS_L	27 28
PPA543	MIPI_CLK_N	27 28
PPA544	MIPI_DATA_N	27 28
PPA545	PCH_BT_UART_CTS_L	17 26
PPA546	PCH_BT_UART_R2D	17 26
PPA548	PCIE_CAMERA_D2R_N	16 28
PPA549	PCIE_CLK100M_SSD_N	16 54 63
PPA551	PCIE_SSD_D2R_N<0>	16 63
PPA552	PCIE_SSD_D2R_P<0>	16 63
PPA560	SMC_BT_PWR_EN	25 30
PPA562	SMC_OOB1_R2D_L	30 59
PPA563	SMC_PROCHOT	30 31
PPA564	SMC_SENSOR_PWR_EN	30 32 34
PPA565	SMC_WAKE_SCI_L	15 30
PPA566	SMC_WIFI_PWR_EN	25 30
PPA567	AP_PCIE_WAKE_L	18 25
PPA569	SSD_SR_EN_L	15 59
PPA570	SYSCLK_CLK12M_SMC	18 30
PPA571	SYSCLK_CLK24M_SSD	18 54
PPA572	SYSCLK_CLK24M_CAMERA	18 27 65
PPA575	TPAD_SPI_CS_L	17 29
PPA576	TPAD_SPI_INT_L	17 29
PPA577	USB3_EXTA_D2R_N	16 60
PPA578	USB3_EXTA_D2R_P	16 60
PPA579	CPU_CATERR_L	6 30
PPA581	MEM_B_CS_L<1>	7 22
PPA582	MEM_B_CKE<1>	7 22
PPA583	MEM_B_CAB<1>	7 22
PPA584	MEM_B_CAA<2>	7 22
PPA587	MEM_B_CAA<3>	7 22
PPA594	XDP_USB_EXTA_OC_L	16 23 24 63
PPA596	USB_EXTA_P	16 23
PPA597	USB_EXTA_N	16 23
PPA598	PM_DSW_PWRGD	15 30
PPA500	AP_CLKREQ_L	16 25
PPA501	AP_RESET_L	14 25
PPA502	CAMERA_CLKREQ_L	16 27
PPA503	CAMERA_RESET_L	14 27
PPA521	CHGR_BOOST_DH	41
PPA586	CHGR_BOOST_DL	41
PPA524	CHGR_BUCK_DH	41
PPA525	CHGR_BUCK_DL	41
PPA526	CPUCORE_FCCM	42 43
PPA527	CPUGT_FCCM	42 44
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PPA532	CPUCORE_PWM1	42 43
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PPA536	CPUGT_PWM1	42 44
PPA540	CPUGT_PWM2	42 44
PPA541	CPUSA_PWM	42 43
PPA542	P1V2_DRVH	47
PPA547	P1V2_DRVL	47
PPA589	PVCCIO_DRVH	47
PPA588	PVCCIO_DRVL	47
PPA550	P1VSUS_DRVH	48
PPA590	P1VSUS_DRVL	48
PPA553	LPC_SERIRQ	14 30
PPA554	SMC_CLK32K	30 31
PPA555	SYSCLK_CLK32K_PCH	16 18
PPA556	SYSCLK_CLK32K_CAMERA_BT_AP	18 25
PPA557	SYSCLK_CLK24M_PCH	16 18 63
PPA558	TPAD_SPI_IF_EN	17 29
PPA559	CPUCORE_GL1	43
PPA561	CPUCORE_GL2	43
PPA568	CPUGT_GL1	44
PPA573	CPUGT_GL2	44
PPA574	SMC_BC_ACOK	30 31 34 41 63
PPA580	P2V7NAND_DRVL	57
PPA585	P1V8SUS_PGOOD	46 48

SSD & WiFi Chamber Test Points

TPA500	PPDCIN_G3H	24 34 41 61 65
TPA501	PPDCIN_G3H	24 34 41 61 65
TPA502	PPDCIN_G3H	24 34 41 61 65
TPA503	PPDCIN_G3H	24 34 41 61 65
TPA504	GND	
TPA505	GND	
TPA506	SMC_ONOFF_L	29 30 31 32
TPA507	SSD_BOOT_L	17 54
TPA508	SMC_DEV_SUPPLY_L	30
TPA509	GND	
TPA510	SMC_DEBUGPRT_TX_L	30 31 65
TPA511	SMC_DEBUGPRT_RX_L	30 31 65
TPA512	SSD_UART_R2D	17 63
TPA513	SSD_UART_D2R	17 63
TPA514	PCIE_TEST_D2R_P	16 65
TPA515	PCIE_TEST_D2R_N	16 65
TPA516	PCIE_TEST_R2D_P	16 65
TPA517	PCIE_TEST_R2D_N	16 65
TPA518	PCIE_CLK100M_TEST_P	16 65
TPA519	PCIE_CLK100M_TEST_N	16 65
TPA520	TEST_CLKREQ_L	16 65
TPA521	PLT_RST_L	5 14 15 19 26 30
TPA522	USB_TEST_P	16 65
TPA523	USB_TEST_N	16 65
TPA524	GND	
TPA525	GND	
TPA526	POWER_GATE_EN	23 24 41
TPA527	PP3V3R3V0_AON	23 41 61
TPA528	HIPWR_EN	23 41
TPA529	PM_SLP_S3_L	15 30 46 49 50 51

65 27 18	SYSCLK_CLK24M_CAMERA	MAKE_BASE=TRUE	SYSCLK_CLK24M_CAMERA	18 27 65
24 23	SMC_UART_TX	TRUE	SMC_DEBUGPRT_TX_L	30 31 65
24 23	SMC_UART_RX	TRUE	SMC_DEBUGPRT_RX_L	30 31 65

NO_TEST Nets

		NO_TEST MAKE_BASE		
65 16	NC_USB3_EXTB_D2RP	TRUE	NC_USB3_EXTB_D2RP	16 65
65 16	NC_USB3_EXTB_D2RN	TRUE	NC_USB3_EXTB_D2RN	16 65
65 16	NC_USB3_EXTB_R2D_CP	TRUE	NC_USB3_EXTB_R2D_CP	16 60 CPU/PCH
65 16	NC_USB3_EXTB_R2D_CN	TRUE	NC_USB3_EXTB_R2D_CN	16 65
65 16	NC_USB_EXTBP	TRUE	NC_USB_EXTBP	16 65
65 16	NC_USB_EXTBN	TRUE	NC_USB_EXTBN	16 65
65 16	NC_USB3_EXTC_D2RP	TRUE	NC_USB3_EXTC_D2RP	16 65
65 16	NC_USB3_EXTC_D2RN	TRUE	NC_USB3_EXTC_D2RN	16 65
65 16	NC_USB3_EXTC_R2D_CP	TRUE	NC_USB3_EXTC_R2D_CP	16 65
65 16	NC_USB3_EXTC_R2D_CN	TRUE	NC_USB3_EXTC_R2D_CN	16 65
65 16	NC_USB_EXTCP	TRUE	NC_USB_EXTCP	16 65
65 16	NC_USB_EXTCN	TRUE	NC_USB_EXTCN	16 65
65 16	NC_USB3_EXTD_D2RP	TRUE	NC_USB3_EXTD_D2RP	16 65
65 16	NC_USB3_EXTD_D2RN	TRUE	NC_USB3_EXTD_D2RN	16 65
65 16	NC_USB3_EXTD_R2D_CP	TRUE	NC_USB3_EXTD_R2D_CP	16 65
65 16	NC_USB3_EXTD_R2D_CN	TRUE	NC_USB3_EXTD_R2D_CN	16 65
65 16	NC_USB_EXTDP	TRUE	NC_USB_EXTDP	16 65
65 16	NC_USB_EXTDN	TRUE	NC_USB_EXTDN	16 65

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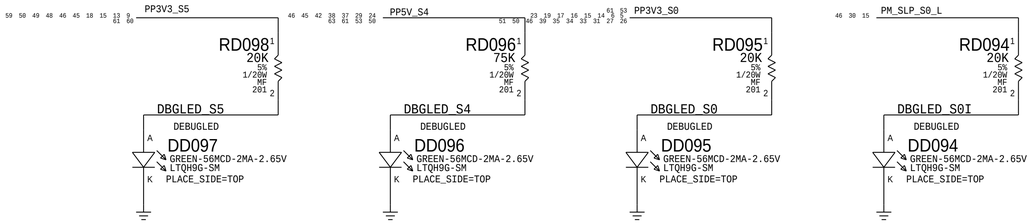

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